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Review on Parameter Optimization of Inductive Source Degeneration Low Noise Amplifier

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Abstract

This article examines the current status of low-noise amplifiers (LNAs) and their vital role in amplifying weak signals in various applications. The study also examines the various technological advancements made in the field of low-noise amplifier design circuits. In the past couple of decades, the design and optimization of CMOS LNA with the help of nature-inspired techniques has gained widespread attention. Various optimization methods, like evolutionary algorithms and swarm intelligence, have improved a device's noise figure, power consumption, and gain. This work presents an overview of the different design techniques for LNA based on the cascode inductive source degeneration topology with the help of CMOS (Complementary Metal Oxide Semiconductor) technology. This work presents the recent developments in the design of LNAs optimized for operation in different frequency bands. The literature lists various design methods and techniques for optimizing the LNA's parameters through hybrid algorithms. It is often challenging to determine the most suitable approach for a specific situation.

Keywords: LNA, CMOS, Inductive Source Degeneration, Cascade, NF

1 Introduction

In analog integrated circuits, the LNA is a vital component. The automation and design aspects of complex, integrated analog electronic circuits incorporating LNA are still in their early stages, compared to those of digital systems. Researchers also face challenges when developing high-frequency analog Circuits [1].LNA is a type of amplifier that amplifies the

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weak signal often trapped by the antenna of a radio receiver. It is commonly used in wireless communication systems. Just after the receiver's antenna, the LNA is the major element that determines the overall system noise and linearity of a radio frequency receiver. It is a sensitive block and plays a crucial role in enhancing the receiver's performance. The LNA is primarily used in the receiver to amplify the weak signal that the antenna sends out. It can then extract the signal from the environment that's undesirable, allowing the block to advance down the chain and process the signal [2].

The LNA is a critical component, as it dominates the sensitivity. Due to its design, there are various tradeoffs between linearity, gain, NF (Noise Figure), power dissipation, etc. The objective of the low-noise amplifier design is to provide input matching and noise at the same power dissipation level. An LNA is designed to provide sufficient gain to control the noise generated by the receiver during various operations. It is also intended to reduce the overall system noise level. For most receivers, this component is the first step in the link between the antenna and the duplexer. The performance of the LNA significantly affects the system's overall noise level and gain [3].

An LNA is also designed to amplify a signal with a suitable NF. The ideal LNA should have a high gain, 1 dB P1dB compression point, bandwidth, and IIP3 (third order input intercept point) specifications. It should also have a low area, power consumption, and NF [4].

The advancement of CMOS technology has greatly contributed to the development of wireless communication. It has allowed the various components of wireless systems, such as RF (Radio Frequency) oscillators, detectors, and front-ends, to perform better and more efficiently. This overview will cover the key aspects of the CMOS technology's importance. The signal integrity of complex systems can be maintained by the synchronization of data communication and clocks using a CMOS phase detector [5]. The high integration density, small size, low power consumption, and low cost of CMOS are some of the advantages that make it a popular choice for various applications in the radio frequency industry.

The following sections show the various parts of this paper: section (2) Basic Building Block of RF-LNA (Radio Frequency Low Noise Amplifier), section (3) Inductive Source Degeneration, section (4) Single-Ended LNA, section (5) Literature Survey on Optimization-based Techniques, and section (6) finally the Conclusion.

2 Basic Building Block of RF-LNA

The LNA serves as the fundamental block of a receiver system. When weak signals are received by a radio frequency receiver, it amplifies them using the LNA. A fundamental building block of an RF-LNA consists of a band-pass filter and a low-noise amplifier. The initial signal received by an RF receiver is sent to a BPF (band pass filter). After considering the receiver's antenna, the band-pass filter forwards the weak signal containing noise to the LNA [6].

A noise figure is computed by considering the receiver's initial condition. An LNA plays a vital role in electronic devices by amplifying the incoming signal and reducing its noise through various stages [7]. While an LNA is primarily designed to amplify a weak signal, it must also add distortion and low noise to boost its reference power. These components can provide the receiver with additional information once it has received the transmitted Signal.

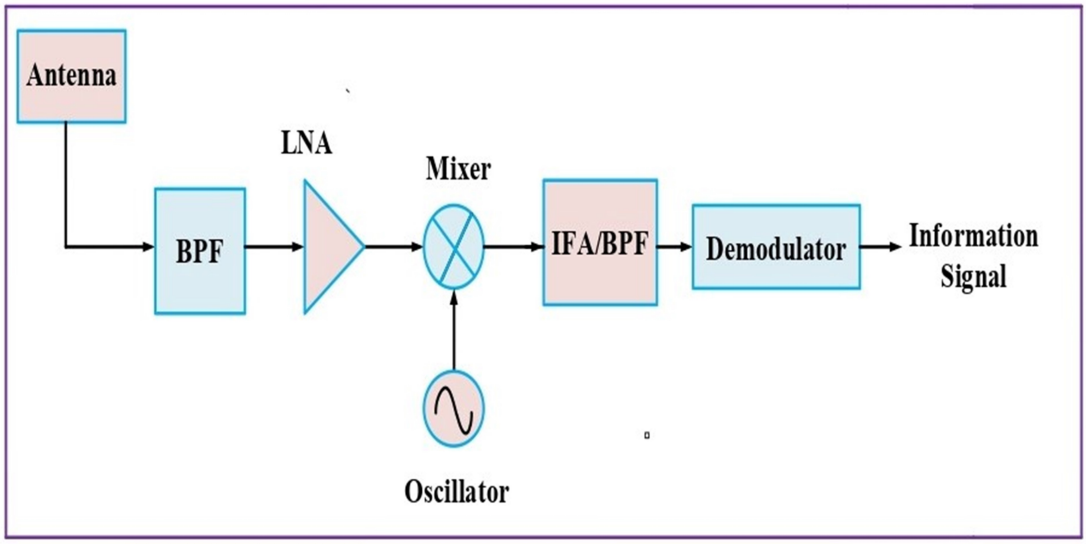

Fig. 1: Basic Block Diagram of RF-LNA [8]

3 Inductive Source Degeneration

Inductive Source Degeneration LNA offers a negative series feedback, which reduces the gain of the amplifier. Moreover, it offers an additional degree of freedom in controlling the input impedance, the optimal source impedance, and the minimum noise figure of amplifiers. Also, since it does not include noise, the concept of inductive degeneration is highly attractive. The input impedance of an amplifier can be affected by the implementation of L_s and inductive source deterioration in the common-source amplifier .

$$Z_{in} = R_l + R_c + R_s + \frac{g_m L_s}{C_{gs}} + j\omega L_s + \frac{(1 + g_m R_s)}{j\omega C_{gs}} \tag{1}$$

$$Z_{in} = R_l + R_c + \frac{1}{j\omega C_{gs}} + \left(1 + \frac{g_m}{j\omega C_{gs}} \cdot \frac{Z_o}{Z_o + Z_L}\right)((R_s + Z_s) \,//\, (Z_o + Z_L)) \tag{2}$$

Where load and the degeneration impedances are represented by Z_L and Z_s, respectively. A simulation was performed to analyze the effects of varying values of the inductive source degeneration (L_s) on the input return loss [9].

Various types of input circuits can be used in single-ended topologies. These include the resistive termination common source, the shunt-series feedback, the common gate, the $1/g_m$ termination, the inductive common source, and the cascode inductor source degeneration. Using resistors to generate an impedance matching circuit has limitations. Unfortunately, the noise performance of the LNA devices is negatively affected by the resistive components. The common gate circuit has a lower gain than the other designs, which is a disadvantage when it comes to low power consumption. In addition, the noise figure of the $1/g_m$ termination architecture can go up to around 3 dB.

The LNA devices built using inductors are more noise-efficient than their counterparts using resistors. The cascode source degeneration topology among these architectures

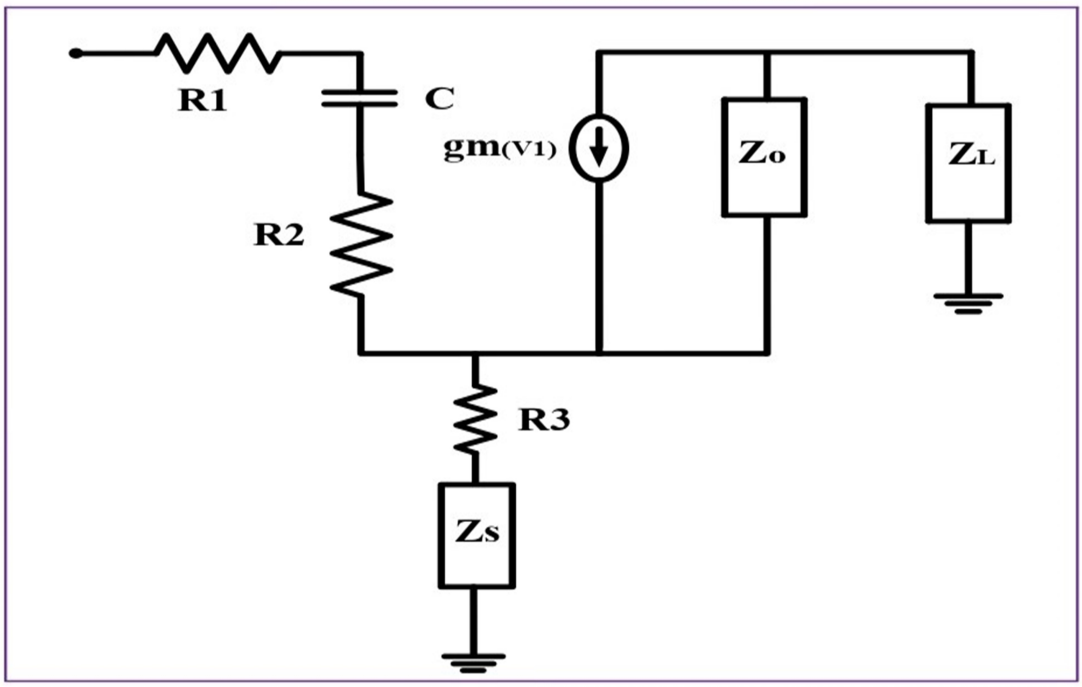

Fig. 2: Basic Block Diagram of RF-LNA [9]

has the best performance when it comes to output and input isolation, noise factor, and gain. The input and output terminals are equipped with inductors that match the off-chip impedance. The tank circuit is also built with output capacitance and drain inductors. The disadvantages of the cascade design are its larger size compared to other single-ended designs, topology, and the use of off-chip inductors [10].

The design of an LNA is important because it should have sufficient gain to deliver low power levels without degrading the SNR. It should deliver strong signals with low power consumption and low distortions. Numerous LNA architecture concepts are presented each year. Unfortunately, there's no standard LNA topology that's suitable for every type of application. To get the most out of its potential, some of its properties must be sacrificed to achieve optimal results. The trade-offs between various LNA design architectures are shown in Figure 4 below.

The performance parameters of an LNA are also taken into account to determine its efficiency. Some of these include the gain, noise figure, power consumption, input reflection coefficient (S_{11}), output reflection coefficient (S_{22}), forward transmission (S_{21}), reverse transmission (S_{12}), third-order input intercept point (IIP3), and system stability. To maximize the design's performance, inevitable trade-offs must be considered. This applies to sensitive RF components since varying parameters could affect the behavior of others. Priority is given to certain parameters. For instance, stability should never fall below one to avoid a potentially unstable circuit.

During a simulation of a circuit, the consequences of an issue with the output resistor were detected. For instance, it is recommended to remove the output resistor to prevent the gain from decreasing. In addition, tuning is performed to maintain the k-factor stability

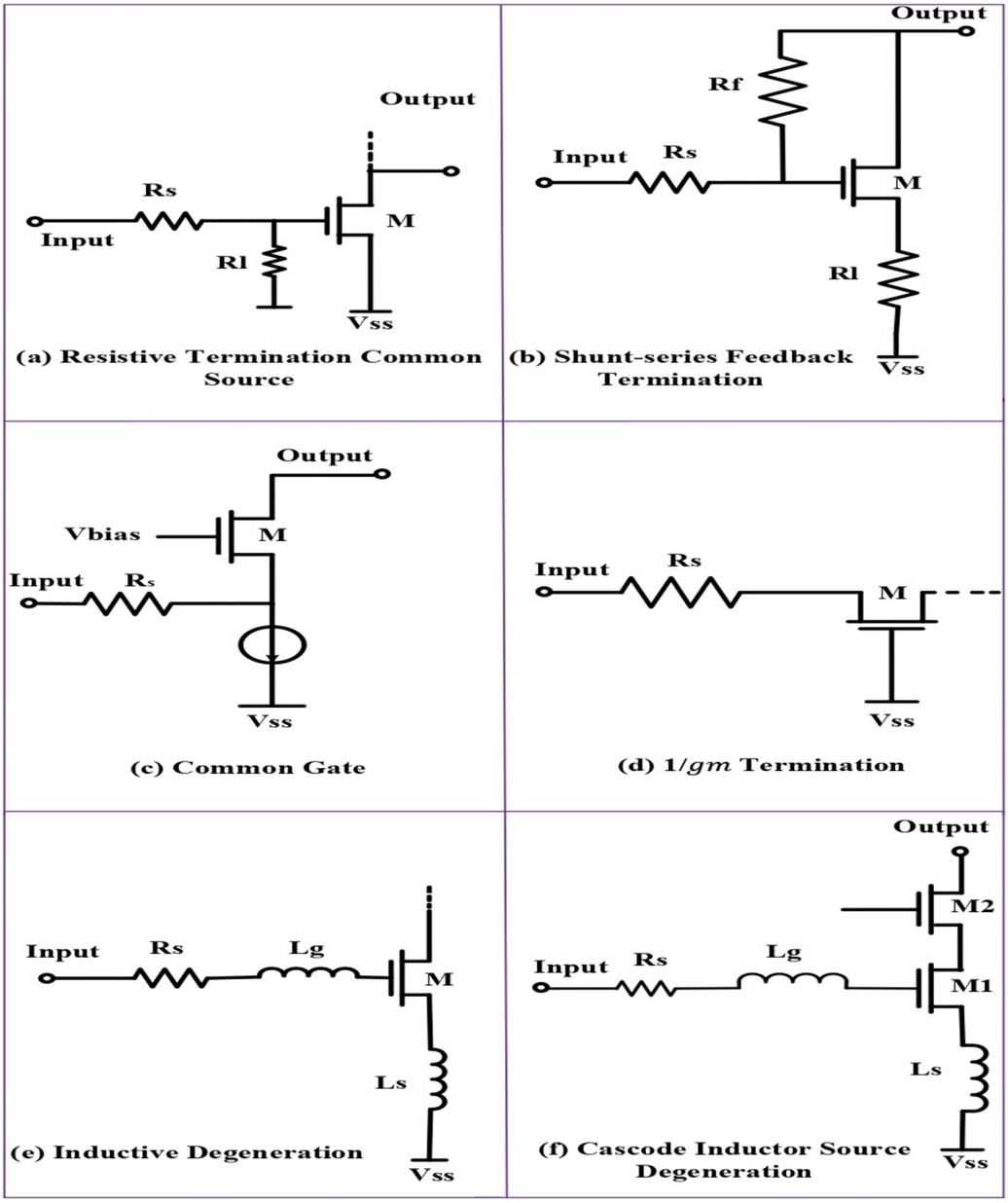

Fig. 3: Basic Block Diagram of RF-LNA [10]

of the LNA higher than its unity. The output matching network of an LNA is usually designed to provide maximum gain with conjugate matching [11]. In addition to this, the trade-off between linearity and high gain should be considered. The power consumption and the gain of a circuit should also be considered simultaneously.

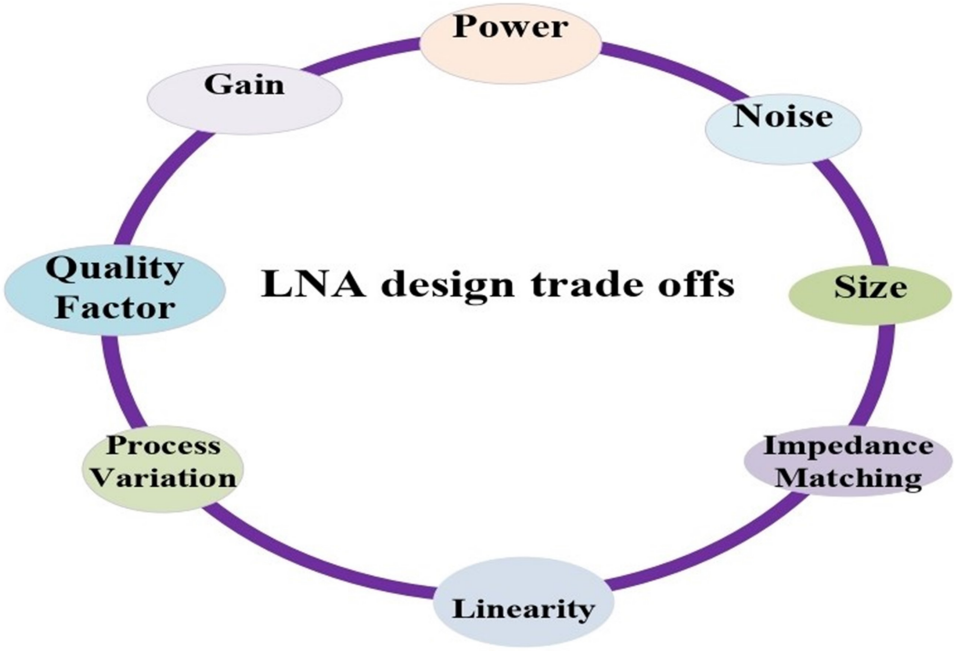

Fig. 4: Basic Block Diagram of RF-LNA [10]

4 Single-Ended LNA

One of the popular types of LNA architectures is the single-ended LNA, which has been proven to offer high isolation, high gain, and good noise performance. The single-ended LNA architecture utilizes a cascode inductive source degeneration. The connection of the transistor to the gate leads to a reduction in the Miller Effect capacitance. This type of structure utilizes an inductor L_s that's connected to the M_1 transistor's source. The real component of the input impedance can only be determined by selecting the correct L_s. The transistor M_2's function is to minimize the effects of the tuned input [12].

The primary LNA performance parameters of interest are:

- Noise Figure (NF)
- Voltage Gain
- Input and Output Reflection coefficient (S_{11}, S_{22})
- Power Consumption (P)
- Reverse and Forward Transmission (S_{21}, S_{12})
- Stability (K)
- Third-order Input Intercept Point (IIP3)

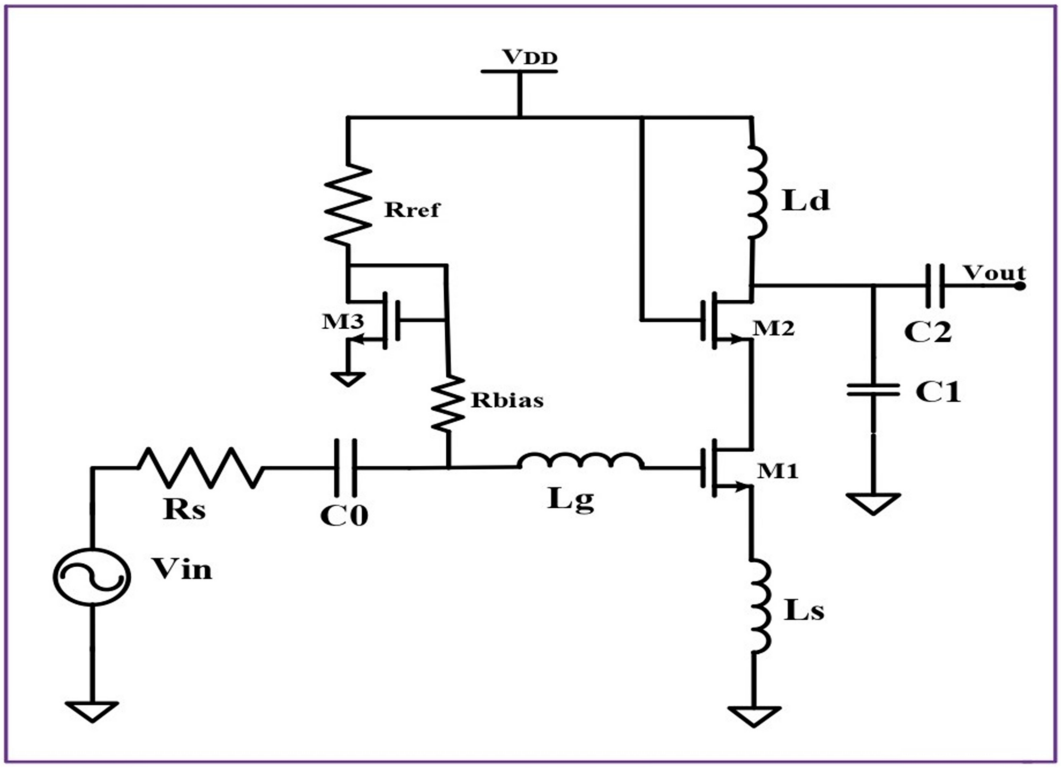

Fig. 5: Basic Block Diagram of RF-LNA [13]

5 Literature Survey on Optimization-Based Techniques

The use of nature-inspired algorithms in the design and optimization of CMOS LNAs has gained widespread attention. Various techniques, such as evolutionary algorithms and swarm intelligence, have been utilized to enhance the performance of gain, noise figures, and power consumption in these devices. The optimization of LNA parameters can help improve the performance of certain applications. Today, optimization plays a vital role in scientific and engineering applications. The global optimization method introduced by the multi-objective algorithm seeks to boost the global convergence process. Recent studies have revealed several methods that can help achieve better noise figures and overall LNA design efficiency. Multi-objective optimization techniques and performance evaluations are utilized to address the issue of optimizing the size of integrated circuits (ICs).

The process of optimization involves generating new design parameters for each iteration. These include the length and width of transistors, the size of the resistors, the inductors, the capacitors, and the other components. The two objective functions of an LNA are the noise figure and the voltage gain, which are both optimized through MOPSO (multi-objective particle swarm optimization) and MOABC (multi-objective artificial bee colony) optimization techniques. It is important to maximize the voltage gain and minimize the noise figure to achieve a good deal while still meeting the design constraints of the target specifications. The dual optimization of the noise figure and voltage gains of an LNA circuit is carried out through the application of the MOPSO and MOABC algorithms.

The main objective is to achieve an optimal trade-off between the noise figure and the voltage gain, i.e., to maximize the voltage gain (Gain = 21.200 dB) and minimize the noise figure (NF = 0.848 dB) in addition to consuming less power. The MOABC and MOPSO algorithms were used to generate the optimal Pareto front. The ADS (advance design system) simulator is utilized to simulate and evaluate the LNA circuit specifications and performances. The ADS simulator's design parameters are based on the MOPSO and the MOABC algorithms. The simulations were performed with a 1.8 V power supply using the 180-nanometer CMOS technology. The optimized design was implemented in the 180-nanometer CMOS technology, which is supported by a 1.8 V power supply and operates at the 2.4 GHz frequency. Compared to the previous optimization techniques, the LNA that was designed performed better. The noise level generated by the Cascode M_2 transistor is insignificant. In addition, the bulk resistance and source noise are not considered in the analysis [14].

The optimization of LNA parameters (noise figure, gain, and linearity) is a common problem in electrical and electronics engineering. It involves simultaneously optimizing different objectives. Since it is a multi-objective process, a deep level of expertise is required to select the best tradeoff. The Firefly Algorithm is a promising multi-objective algorithm from a meta-heuristic family that can be used to solve the various optimization problems related to the design of LNA parameters. Due to its multi-objective design, it can perform simultaneous optimizations of the input and output parameters, as well as the Gain, noise figure, and linearity. The designed CMOS LNA circuit is based on a 5.5 GHz frequency and utilizes three spiral inductors, which are on-chip. These are drain inductor (L_d), gate inductor (L_g), and source inductor (L_s). The Firefly Algorithm (FA) is the multi-objective algorithm used to enhance the performance of the 5.5 GHz LNA. To enhance the convergence process, a multi-objective algorithm that is based on the direct global optimization method is used. Five design variables, gain or S_{21} (dB), Noise Figure (NF (dB)), third order input intercept point (IIP3), input reflection coefficient (S_{11} (dB)), & output reflection coefficient (S_{22} (dB)) are optimized. The preferred constraints for optimal input and output matching are L_g and L_s.

To optimize the performance structures of inductive source degeneration LNA focused on enhancing the structure's noise figure, gain, linearity, and matching. For instance, the size of M_1 should be 229 μm while that of M_2 should be less than the value of M_1. Using the Firefly Algorithm for optimizing a 5.5 GHz LNA is a significant advance in the field of circuit design. It helps in balancing various performance metrics, such as the noise figure and gain. This is part of a trend toward utilizing nature-inspired approaches in optimizing electronic circuits. The designed inductive source degenerated LNA is implemented & simulated using the UMC 180nm CMOS technology in the CADENCE simulator tool. It accomplishes the optimization of LNA parameters, like gain, linearity, noise figure, and input & output matching. The designed LNA achieved a simulated value of the optimized LNA of gain of 22.15 dB, IIP3 of -2.60 dBm, noise figure (NF) of 1.168dB, and 5.5 GHz frequency. The optimized LNA parameters with the help of the FA algorithm achieved IIP3 of 0.356dBm, NF of 1.24dB, gain of 23.01 dB, an input reflection coefficient of -26.56dB, and an output reflection coefficient of -18.18 dB [15].

A swarm-based optimization algorithm known as the firefly algorithm is utilized to design a low noise amplifier and enhance the performance parameters of an LNA, specifically the maximization of gain and minimization of noise figures. In two case studies, the optimization of both NF and gain was considered. The optimization of the two parameters

by considering them as single objective functions, and the penalty factor technique is used to manage the constraints. The other LNA parameters, such as linearity, stability, and power consumption, are also optimized. It is the first time that the FA has been used to comprehensively optimize the LNA parameters. The LNA was designed using an inductive-source degeneration structure and is implemented using the 0.18-μm CMOS technology with the help of the CADENCE software and MATLAB environments. The designed LNA achieves an optimized noise figure of 0.4811 dB with the FA technique, which is significantly lower than the other algorithms, and an optimized gain of 23.508 dB, which is higher than the other algorithms. The FA has a significantly better computational efficiency than modern algorithms. The Firefly algorithm to optimize the LNA parameters performed better than the other widely used optimization algorithms, such as the backtracking search algorithm (BSA), human behavior PSO (HB PSO), particle swarm optimization (PSO), and cuckoo search algorithm (CSA), in terms of their computational efficiency, robustness, and consistency [16].

For RF applications, improve the efficiency of the cascode common-source low noise amplifier by incorporating an inductive source degeneration topology. A novel structure that can increase the power gain (S_{21}) of a typical cascode common-source LNA using inductive-source degeneration. This novel LNA, which utilizes an additive capacitor and transistor, has a better figure-of-merit (FOM) and lower noise figure (NF) than the conventional cascode common-source LNA. For enhanced power gain, an innovative structure to improve the efficiency of the common-sourced LNA with an induction source degeneration process. The proposed LNA utilizes a capacitor and a transistor, which is more than what's found in the conventional type. It also improves the third-order input intercept point (IIP3) of the LNA through the use of a capacitor. The minimal noise figure achieved by the UWB-LNA technology is slightly lower than that of the conventional LNA [17].

A one-stage cascode source inductive degeneration LNA has been designed, which is based on 130-nanometer technology, for 18 GHz. It can achieve high linearity, good noise figures, a suitable S-parameter, and low power consumption. The various simulation techniques, such as the genetic algorithm, the simulated annealing method, and Levenberg Marquardt, simultaneously optimize the design specifications, such as the noise figure, S-parameters, and the third-order input intercept point in the process. The 15.8 FOM of the LNA made it suitable for use in the frequency range of operation of the various CMOS LNAs that are commonly used. The optimized simulation of the proposed LNA revealed that it has an NF of 1.8 dB for a frequency (f) of 17.49GHz. The input reflection coefficient (S_{11}), the output reflection coefficient (S_{22}), and the reverse reflection coefficient (S_{12}) of the LNA were also noted at -12.84 dB, -8.48 dB, and -30 dB, respectively. The maximum available gain and maximum stable gain of the proposed LNA for 17.49 GHz frequency are 18.6 dB and 23.75 dB, respectively. It has been found that the third-order input intercept point (IIP3) is +11 dBm, the third-order output interception points (OIP3)+23 dBm, and $P_{1\text{dBm}}$ -8 dBm. A statistical and evolutionary simulation-based approach for designing a high-gain CMOS low noise amplifier for 18 GHz using 0.13-micrometer technology. The LNA achieves a noise figure of 1.8 dB at the peak of its gain frequency at 17.49 GHz. The optimized LNA performed well in various aspects such as linearity, gain, and noise figure (NF) [18].

Performance analysis of the low-power LNA provides the design method for a wide-band LNA utilizing the PSO technique. It explores the low power enhancement and low voltage of the LNA design for this type of application. In addition, a biasing metric was

developed based on the experiments conducted with LP (Low Power) and LV (Low Voltage) analog circuits. The LNA was then divided into two phases: the CS (common source) and the current reuse topology. The first phase featured a group of top PMOS and NMOS transistors, which took into account the inductive sequence peaking in the feedback loop. It is a low-power, low-voltage LNA optimized for wideband applications. It can also achieve low NF and high gain by implementing a novel PSO and biasing metric. The designed LNA can achieve a maximum voltage gain of 18.57 dB and a low NF of 2.4 dB at 25.4 GHz, and also achieves S_{11} of 17.1dB, S_{21} of 16.6dB at 0.8V and 1.6mW LNA. The design challenges of LV and LP circuits were analyzed using the biasing metric for optimizing the RF analog circuits [19].

Table 1: Comparison of Optimization Techniques for CMOS LNA Design

Ref.	**Techniques Used**	**Design**	**Technology**	**NF (dB)**	**Gain (dB)**
[15]	Firefly Algorithm	5.5-GHz CMOS LNA	UMC 0.18 μm CMOS	0.4811	23.508
[14]	MOPSO, MOABC	LNA Circuit	180-nm CMOS	0.848	21.2
[16]	Firefly Algorithm	5.5-GHz Low-Noise Amplifier	UMC 0.18 μm CMOS	1.24	23.01
[18]	Modified Genetic Algorithm	High-Gain CMOS LNA	0.13 μm CMOS	1.8	23.75
[19]	Particle Swarm Optimization (PSO)	Low-Power LNA	–	2.4	18.57
[20]	Particle Swarm Optimization (PSO)	Current-Reused LNA Design	PVT Variations	1.8	12.52
[21]	Gain-Boosted and Noise-Optimized Technique	CMOS Wide-Band Low-Voltage LNA	0.18 μm RF CMOS	4.2	15.0
[22]	Particle Swarm Optimization (PSO)	LNA Design for UWB Applications	45-nm CMOS	1.89	16.8
[23]	MOIPO	Low-Noise and Efficient LNA Design	180-nm Process	3.8	13.0

The optimal design of the ultra-wideband 2.5 to 10.5 gigahertz LNA using 180-nanometer and 65-nanometer RF (radio frequency) CMOS technology is proposed. The suggested UWB-LNA achieves its optimal performance through two heuristic multi-objective optimization techniques that take into account the optimization methods offered

by PSO and IPO. This UWB-LNA (Ultra-Wide-Band- Low Noise Amplifier) has been designed and simulated through the use of CADENCE Spectre RF and HSPICE tools. The design objectives suggested by UWB LNA designs are frequency band, power gain (S_{21}), NF, power consumption (P_c), input reflection coefficient (S_{11}), and the sum of the inductance values. In the 180-nanometer CMOS technology, the optimized LNA designs by MOPSO and MOIPO utilize a power supply of 1.8 V and consume around 7mW and 7.2mW respectively. On the other hand, in 65-nanometer CMOS technology, both the MOPSO & the MOIPO consume about 10.5mW and 9.5mW, respectively. The results of the 180 nanometer CMOS technology demonstrate a mean S_{21} of 12.47 dB and a standard deviation of 0.18. The NF of 4.01 dB with varying standard deviations of 0.03, and the S_{11} of -22.04 dB with varying standard deviations of 0.94, respectively. In 65-nanometer CMOS technology demonstrates a mean S_{21} of 14.63 dB with a varying standard deviation of 0.19, an NF of 2.55 dB with a varying standard deviation of 0.01, and an S_{11} of -20.15 dB, with a varying standard deviation of 0.91. The optimized UWB-LNA design using MOIPO for 65-nanometer CMOS technology has better performance in terms of IIP3, NF, power gain, and other attributes compared to their counterparts with advanced technologies. An optimal design for an ultra-wideband LNA using a multi-objective optimization technique is used in wideband UWB applications with low NF, low power consumption, and flat power gain. It can achieve this through the use of the Heuristic multi-objective optimization technique and the implementation of novel techniques for power reduction, low noise figure (NF), and broadband matching. It is also able to achieve an input return loss of < -10 dB and a noise figure (NF) of less than 5 dB in 180-nm CMOS technology [24].

The development of automated methods for optimizing low-noise CMOS analog amplifiers has become a critical area of research. This field is focused on minimizing power consumption and optimizing performance. The ALCPSO (aging leader particle swarm optimization) optimization algorithm provides a robust understanding of these goals. The design methodology for the ALCPSO architecture is carried out using MATLAB software and linked to a computer-aided design tool known as CADENCE, with 0.18 μm technology, which is capable of verifying the algorithm's accuracy. The length of the two MOS transistors, M_1 and M_3, is a design parameter variable. The main objective function of the design procedure carried out using the ALCPSO framework is to minimize total area and thermal noise. The cost function optimization process consists of two steps: the first one deals with the minimization of thermal noise. The other one involves the optimization of the other design specifications. The design methodology implemented by the ALCPSO algorithm can achieve various optimal parameters of a low-noise CMOS analog amplifier, such as the total circuit area of 87.346 μm^2, taking a minimum time of around 0.7354 seconds, and the thermal noise level of 21.26 $nV/Hz^{1/2}$. The ALCPSO algorithm is used to automatically size and optimize a low-noise digital amplifier by the use of particle swarm optimization in the LNA with its aging leader and challenger's control (ALC) strategy. It is utilized for automating the sizing of CMOS analog amplifiers and explains how an automated approach for designing low-noise CMOS amplifiers can be achieved through ALCPSO optimization. This method is an ideal choice for developing low-noise analog circuits. The algorithm, known as ALCPSO, can be used to address the total circuit area and thermal noise while still meeting the constraints. It was found that the ALCPSO design methodology was able to achieve the optimal solution for low-noise amplifiers. It outperformed the IPSO-based design process in terms of robustness, cost, and performance. The goal of the automated approach is to enhance the design process performance, cost, and

robustness. Noise can restrict the minimum signal level that a circuit can receive. Noise can restrict the signal level to a certain degree. It also has constraints in the design of a differential amplifier [25].

The use of the PSO algorithm for current-reused LNA design is optimized at 4.4 GHz. The particle swarm optimization algorithm was employed to design an LNA with a voltage gain of 12.52 dB based on PVT (Process, Voltage, and Temperature) variations. It also has a corresponding NF of 1.80 dB, an input return loss of -37 dB, and an output return loss of 42 dB at 4.4GHz frequency. The overall die area of the LNA is 939.5 μm $\times$ 746.83 μm. The operating frequency of the LNA is affected by the PVT (process, voltage, & temperature) variations. The PSO algorithm is utilized for the calibration and tuning of the LNA. The input return loss of the proposed LNA using PVT variations is not optimal at the 4.4 GHz frequency. It can be achieved through the PSO algorithm with a minimum S_{11} (input return loss) of -37 dB. The voltage gain (A_v) of the LNA is 12.45 with a PVT variation of ± 0.4 dB without using the PSO algorithm. The output return loss of the proposed LNA at the 4.4 GHz frequency is -35 dB. The voltage gain of the proposed LNA using the PSO algorithm is flat, and it attained a flatness of 12.5 ± 0.02 dB and a peak voltage gain of 12.52 dB while using a 4.4 GHz operating frequency. The variations in the noise figure are found in the range of 3 to 7.7 dB at frequencies varying from 4 to 6 GHz. With the use of the PSO algorithm, a minimum noise figure of 1.8 dB is achieved. With the use of the PSO algorithm, an optimization of around 7 dB can be achieved. The PSO algorithm was utilized for the optimization of the current-reused LNA. The PSO algorithm for their tunable narrow-band LNA was optimized at 4.4 GHz. It can achieve a voltage gain of 12.52 dB and an NF of 1.80 dB. Its input return loss is -37 dB, & output return loss is -42 dB [20].

The new nonlinear method, which is based on a negative image synthesis, can improve the performance of a wide-band microwave amplifier. The different properties of the device were analyzed and investigated using this method. This utilized a combination of the nonlinear and the LNA transistor models and a negative image synthesis method to develop a matching system for the input phase of an amplifier. The design parameters of the three components of the LNA were then analyzed using a nonlinear technique. To improve the LNA's performance, the authors have developed various control techniques. The researchers utilized the Negative Image Synthesis method to design a wideband microwave amplifier. It can incorporate a nonlinear transistor model, minimal passive components, and an optimized matching network. A wideband microwave amplifier with a negative image synthesis has been fabricated by the researchers. It achieved includes an excellent transducer gain, a low noise figure, and an optimized VSWR. The design for an amplifier with a transducer gain of around 10 to 20 dB over frequencies ranging from 1 to 5 GHz has an NF of $<$ 1dB [26].

A new low-noise amplifier based on CMOS technology has been developed that utilizes a gain-enhancing and negative feedback technique to enhance the high-frequency gain. The operating frequency of the designed LNA for use in wideband applications is between 1.5 GHz and 3.5 GHz. It can achieve high bandwidth and high gain by boosting its frequency gain. The different noise-optimized and gain-enhancing techniques create a new low-voltage amplifier for applications that require ultra-wideband power. It can achieve high bandwidth and high gain by boosting its frequency gain. It can provide high gain and low gain while maintaining the same performance. The developed LNA's NF is $<$ 4.2 decibels. Its power dissipation is 8 mW at 1 V supply, 15 dB gain, and the input third-order

IIP3 of 7 dB make it ideal for various applications. This technology can be used to enhance the performance of wireless sensor networks and ultra-wideband networks. A poor noise figure is typically experienced in common-source amplifiers with a resistive-shunt feedback circuit. The tradeoff between the wide bandwidth and high gain is known to cause the noise figure of this type of amplifier [21].

The PSO algorithm and multi-stage noise matching techniques are utilized for the optimization of the LNA in UWB applications. An optimization technique that targets the minimization of high-band noise has been implemented at the cost of increasing the minimum NF. The PSO algorithm is utilized for optimizing the various aspect ratios and passive elements of the LNA. The objective function of this algorithm is the NF and the voltage gain term. The LNA was to be optimized using the PSO with a multi-stage matching technique and achieved a power gain of 16.8dB, a minimum NF of 1.89dB, and an input reflection coefficient of -19.2 dB. The power consumption of this LNA is 32 mW, and its chip area is $2.2\text{mm} \times 1.6\text{mm}$. In terms of its layout design, its core area is 650 μm. The PSO algorithm was utilized for optimizing the LNA for use in UWB applications. Simulations were performed in 45 nm technology with a frequency band of 1 to 20 GHz. In conventional methods, the use of impedance matching cannot reduce the noise figure sufficiently. The suggested approach involves increasing the minimum NF level [22].

The Firefly algorithm has been utilized for optimizing the two-stage Op-Amp performance. An optimization algorithm that is inspired by nature is typically simple, efficient, and has an organized computational framework to optimize the design of analog circuits. Due to the numerous competitive requirements, it is important that the designers thoroughly analyze the various trade-off factors between multiple specifications to achieve the best possible performance. An algorithm was recently implemented in a UMC 180 nm CMOS technique using the CADENCE VIRTUOSO simulator software. It was able to achieve better design parameters than traditional methods. It achieved better results in the slew rate, average power, gain, and total area, which were 31.6 V/μs, 109.3uw, 77.66 dB, and 98μm^2 respectively using CADENCE simulator software The design parameters for the Op-Amp were obtained with the help of firefly are I_{bias} (μA) of 25, C_c (pF) of 2, W_1/L_1 of 4/2, W_2/L_2 of 4/2, W_3/L_3 of 4/2, W_4/L_4 of 4/2, W_5/L_5 of 14.5/2, W_6/L_6 of 7.25/2, and W_8/L_8 of 4/2. In order to optimize the design of operational amplifiers, environmental constraints are considered [27].

One of the main challenges in developing LNA designs is the introduction of the latest design methods that can reduce the no of iterations. Through the use of heuristic optimization techniques, we can identify an optimal design for the LNA and also analyze the various trade-offs between its performance parameters. An optimization strategy is employed to evaluate the UWB-LNA's performance. A figure of merit is then used to analyze the performance. The use of MOIPO (Multi-Objective Inclined Planes System Optimization) for multi-objective UWB-LNA optimization is presented. The low-noise and more efficient LNA design has been created for ultra-wideband receiver applications using CMOS technology and heuristic optimization techniques. The ultra-wideband 3 GHz to 10 GHz low noise amplifier UWB-LNA utilizes the multi-objective MOIPO system optimization method. The UWB low noise amplifier technology has been designed to be used with the 180 nm process technology, and it features various optimization techniques such as current reuse, noise cancellation, and inductive peaking. The S_{11} is less than -15dB, S_{21} is 12.5dB, and NF is 3.8 dB. The outputs of the UWB-LNA provide 0.005 W of power consumption at 1.8V voltage [23].

An evaluation of a 0.18 micrometer ultra-wideband LNA using a CMOS technology reveals its crucial role in wireless communication. It shows its ability to enhance signal quality and minimize noise while consuming less power. The design's cascode source degeneration topology can optimize the performance of the receiver. The use of a cascode source degeneration design can help boost weak signals and maintain low noise levels. The output gain of the proposed LNA is 19.79 dB, while the noise figure is 2.03 dB. This indicates that it can effectively amplify weak signals [28].

One of the most common design techniques that can extend the bandwidth of their cascode common-source components is by implementing an inductive-degradation LNA. This methodology addresses the issue of increasing the input-matching bandwidth by implementing dual-resonant S_{11} and extending the gain bandwidth with the help of a transformer-based output network. The Global Foundries 45-nm CMOS process technology has been used to implement an LNA that can boost the 25.5–50 GHz 3-dB gain bandwidth, and return loss bandwidth of 27–46 GHz, minimum noise figure of 2.4 dB, peak gain of 21.2 dB, and peak IIP3 of -9.5 dBm, under the DC power consumption of 25.5 mW. The consistent performance of the design methodology exhibited by the multiple samples was shown to demonstrate its robustness [29].

The design of the high-output matched narrow band and high-gain LNA using an induced degeneration topology has been presented for use in receiver applications. The main objective of low noise amplifiers is to achieve a maximum gain and sufficient noise figure for real-time applications. The design of this LNA was initially studied for its high gain of up to 20 dB, and it was found that the input matching values were up to 25 dB. The design's reverse isolation coefficient was also analyzed. The design of induced degeneration LNAs allows them to increase their overall gain performance by boosting their signal input. The design of the narrowband inducer LNA was performed in the software version of CADENCE virtuoso software. It exhibited a power gain of 16 dB while operating at 90 GHz and a minimum Noise Figure of 2 dB at an operating frequency of 90 GHz. The LNA design is generally good for receiver applications, such as radio receivers [30].

The research in this project presents an innovative LNA design that utilizes two stages input matching stages for low noise amplifiers. It achieves a lossy characteristic of the components by taking advantage of their inherent properties. The design of the two-stage LNA eliminates the challenges and complexity of feedback networks by balancing the stability and minimum noise figures. The integration of the low pass filter into the design provides enhanced performance when it comes to noise-matching networks. An extensive analysis is then introduced to explore the relationship between the different LNA parameters, namely, stability and noise figures, and the internal resistance exhibited by input-matching components. According to the study, an overall reduction in the noise figure of 0.2 dB in the frequency range of operation. The improvement was achieved through the removal of the feedback network in the LNA [31].

The article looks into specific LNA architecture and emphasizes the significance of high gain, input-output synchronization, and low power consumption. Furthermore, it presents an extensive comparison of LNAs employing different frequency ranges, noise performance, and gain, emphasizing the significant technological developments in this area, encompassing innovations in solid-state transistors and vacuum tubes. The various types of LNAs featured in this study exhibit gain ranging from 8.8 dB to 24.6 dB. Noise figures vary from 0.64 dB to 6.9 dB. The different LNAs exhibited different core areas, ranging from 0.1mm^2 to 28×26 mm^2. Their power consumption also varied from 0.5 mW to 33 mW. The study

also presents the Emerging trends and directions in the design of next-generation LNAs for communication systems. The study takes a look at various LNA topologies. Some of these include the two-stage common-source and transformer-based negative feedback networks, as well as the current-reused cascode noise canceling techniques, cascode gm/ID methodology, twice current reused techniques, and hybrid series-shunt LC tank matching [32].

The paper presents an optimized 6.5 GHz CMOS low noise amplifier with the help of the multi-objective optimizer Firefly algorithm. The FA is regarded as a charity when optimizing the noise figure and gain, even though the design constraints are addressed. The five objectives presented in the paper are considered multi-objective optimization. The weighted sum access method is used to modify these goals to a single objective. The designed LNA has a cascode manufacturing process that uses an inductive source demodulation circuit for use in 6.5 GHz LNAs. This method is implemented in the software for the 0.18μm CMOS technology. The paper has conducted a simulation of a 6.5 GHz LNA with the input reflection coefficient of 21dB, output reflection coefficient at -14dB and -14 dB, noise figure at 1.42 dB, and voltage gain at 19.74 dB, and IIP3 of -3 dBm. The optimized LNA using the FA to evaluate the parameters during a simulation in the MATLAB environment has S_{11}, S_{22}, S_{21}, NF, and IIP3, to be -26.46 dB, -18.41 dB, 20.51 dB, 1.29 dB, and 0.325 dBm, respectively. The execution of the FA is related to the optimization of the LNA parameters using similar algorithms such as the PSO and CSA. The consequences thoroughly demonstrate the advantages of the FA over other approaches when it comes to computational proficiency and consistency [33].

The paper presents an inductively-generated cascode topology for a 130 nm CMOS low noise amplifier. It uses a gain enhancement method. A narrow band LNA is designed for WLAN (Wireless Local Area Network) applications with a 2.4GHz operating frequency. The proposed LNA uses the single stage of the cascode LNA procedure to improve the isolation and noise figure. The designed LNA achieves a high increase and low noise figure and great reverse isolation over the recurrence range for good stability. The LNA is organized with an input impedance of 50 Ω and biased with a 1.2V supply voltage. A low noise inductor is integrated at the main transistor drain to reduce the noise level of the cascode transistor. This designed LNA achieves the noise figure, NF of 0.94 dB, S_{11} is -11.36 dB with the power consumption of 12.09mW, and gain, S_{21} of 23.36 dB. The output return loss, S_{22}, is -3.85 dB, and the reverse voltage gain, S_{12}, obtained is -40.61 dB. The simulated IIP3 value for the third input intercept is -14.33 dBm [34].

The optimized parameters for variable gain LNAs are presented by utilizing the PSO, GA, and FA algorithms. The three optimization techniques were evaluated, and the results of the analysis revealed that the FA algorithm is better than the PSO and GA. The Variable Gain LNA is composed of the CCG (Complementary Common Gate) and a VGA (Variable Gain Amplifier). The Gm-improvement topology is advantageous as it increases the gain while also reducing the power consumption of the current reuse method. The simulated results of the optimization techniques were presented in a model with a minimum noise figure of 2.62 dB and a maximum gain of 17.8 dB. The input reflection coefficient of -13.5 dB and the output reflection coefficient of -14.7 dB were also shown. The figure of merit is 36.14 dB with the use of the FA algorithm. The optimized parameters of the FA algorithm were simulated using the GPDK 45 nm CMOS technology with a frequency range of 26 to 32 GHz on the Cadence Virtuoso software. The results indicated that the minimum NF of 2.6 dB and the maximum gain of 16.9 dB were achieved at 30.9 GHz and

30.5 GHz, respectively. The realized circuit's layout area is 231.695 μm $\times$ 164.48 μm, which is equivalent to 0.03811mm^2 [35].

6 Conclusion

We have thoroughly reviewed several algorithms and techniques that were derived from different fields and combine evolutionary and meta-heuristic techniques to enhance the efficiency of the design process of analog electronic circuits, including CMOS low noise amplifier analog devices. This survey covered the various techniques that are utilized in the parameter optimization of analog electronic circuits. These include the optimization of the power consumption robustness, circuit sizing, and sensitivity to variations in their design parameters. The techniques were presented as a strategy to optimize the size and efficiency of low-noise amplifiers. This survey aims to introduce the techniques that are used to improve the efficiency of LNAs by analyzing their power consumption, bandwidth, NF, IIP3, and gain. A cascaded low-noise amplifier can be designed using the Friis noise formula, which involves optimizing two stages. This literature review aims to provide researchers and designers with a quick and comprehensive overview of the features of small signal low-power amplifiers. Most of the reviews on low noise amplifiers focus on describing the topologies of LNAs at high frequencies. Due to the lack of sufficient literature reviews on the design and evolution of small signal LNAs that operate in low frequencies, it is often difficult for researchers to conduct effective studies.

Declarations

- The authors received no specific funding for this study.
- The authors declare that they have no conflicts of interest to report regarding the present study.
- No Human subject or animals are involved in the research.
- All authors have mutually consented to participate.
- All the authors have consented the Journal to publish this paper.
- Authors declare that all the data being used in the design and production cum layout of the manuscript is declared in the manuscript.

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