Performance analysis of single gate strained Si, Si-Ge on insulator MOSFET in TCAD

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Abstract. Scaling of MOSFET is an important part of semiconductor industry and manufacturing of ICs and due to the scaling several issues like mobility degradation and reduction in I_{on}/I_{off} ratio arises. To overcome these problems many structural approaches evolved over the time such as SOI, FDSOI, and multi-gate technology. Also, in this paper N-MOS Strained Si/relaxed $Si_{0.7}$ $Ge_{0.3}$ hetero-structure is modelled and simulated using TCAD. Performance analysis of Strained-Si N-MOSFET has been done in 2D TCAD simulator. The performance of strained silicon is enhanced and analyzed using proper doping, higher work function, and thin high k dielectric oxide layer. The performance of the strained Si simulated device showed better results than the previous studied work.

Keywords: Strain**,** Biaxial tensile Strain, Multi-gate, SOI, DIBL, Work function, Sub-threshold swing.

1. Introduction

With the continuous scaling, the dimensions of transistor when enter in particular regime where the unusual effects begin to degrade the performance of the device. These effects include short channel effects, carrier mobility degradation and sub threshold leakage. Strained silicon is an emerging technology which has potential to improve the device performance. Strain silicon helps in improving the carrier mobility in channel due to which the drive current increases. When thin silicon epitaxial layer is grown on silicon germanium layer result in the mismatch of lattice constant among both materials, the silicon layer undergoes in tensile strain [4] which leads to the tensile strain in silicon layer. Due to strain the valance and conduction energy bands modifies which decreases the inter-valley scattering and carrier effective mass and hence, carrier mobility in strain silicon channel increases. There is 4.17% mismatch in lattice between silicon and germanium. In silicon each energy level is composed of six equal energy states. The divisions of six energy states are as two perpendicular Δ_2 and four parallel to plane Δ_4 states. Before applying strain the electron effective mass in these states is equal. When biaxial strain is applied in silicon these states (Δ_2 and Δ_4) split up into lower and higher energy

states respectively [6]. Due to band alteration the electron reside in lower energy site which is Δ_2. Due to the difference in energy levels the electrons repopulate in lower energy state Δ_2.Theenergy state Δ_2 have lower effective mass of electrons as compared to Δ_4 state. The effective mass of electrons in this lower energy state reduced to $0.19m_o$ in strained silicon as compared to $0.33m_o$ in unstrained silicon. Now, due to this reduction in effective mass the mobility of this electron in strained silicon increases. Due to this the leakage current decreases and drain current (I_{ds}) increases in (I_d-V_g) plot. Previous work on strained silicon focused on the mobility enhancement entirely. In this work single and double gate strained structure were modeled and simulated in Cogenda TCAD simulator. Also, the performance of both the devices is enhanced by modifying different parameter and oxide material. Great improvement was seen in carrier mobility, I_{on}/I_{off} ratio and sub threshold swing in both the devices.

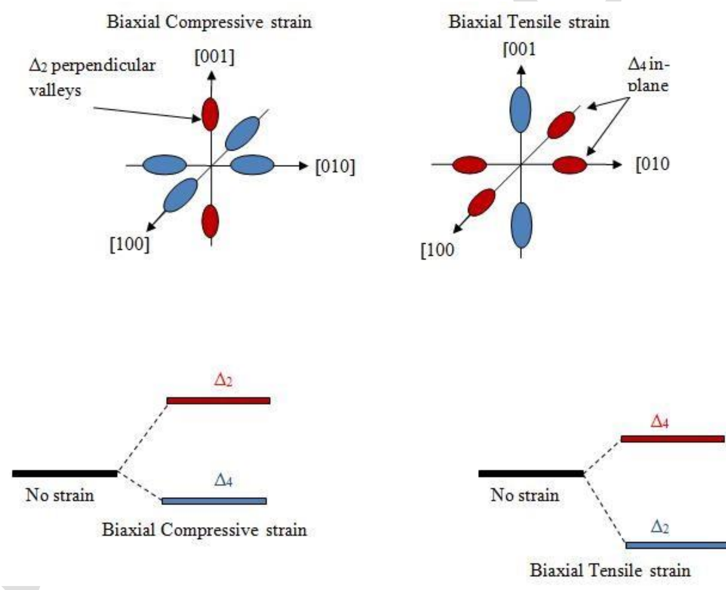

Fig.1.1 Biaxial compressive and tensile strain effect in energy states

2. Research Methodology

The basic aim of this research is to study the performance analysis of strained silicon silicon-germanium-on-insulator structure. This was achieved with the help of Cogenda TCAD v.1.9.2 tool. The designing of the device, simulation and comparison of results have been obtained on this tool. Here the flow of research methodology and the steps for designing device and simulating the design is detailed. The simulation and design parameters used are also detailed.

To ensure proper conduct of the research a methodology needs to be followed. It is the pre- planning of the work that has to be carried out in an ordered manner that is defined in definite steps.

1. To build the proper understanding of the device technology, an extensive literature survey needs to be carried out.
2. Identify the problem areas and the parameters to be worked upon.
3. Decide the technology node and the shape of the device based on which the device has to be constructed.
4. The next step is to design, simulate and extraction of results of the device.
5. Analyze the device with the help of visualizations and compare the results by plotting the I-V characteristics.

Based upon the comparisons drawn, propose the optimized design that provides the better performance of the device.

The flow of research methodology is described in Figure 2.

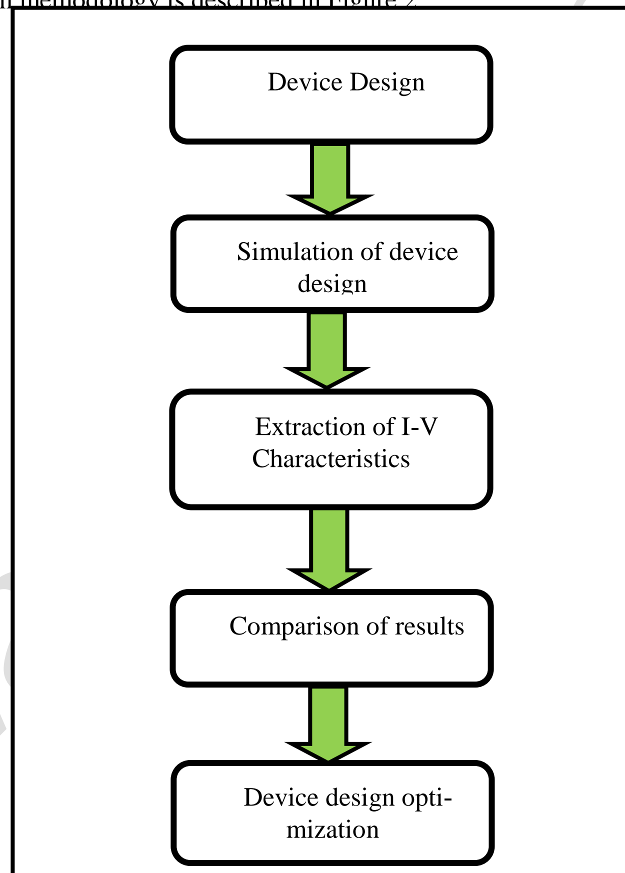

Figure 2.1 Design flow of research methodology

1. **Device Design:** The device can be designed in two ways using Cogenda TCAD tool, depending upon the type of design whether it is 2-D or 3-D design.

   2-D Device Design:

   A two dimensional device is designed by drawing it in Device drawing window. This includes following steps:

   i. Drawing the outline of the structure by making use of boxes, poly-lines, lines etc.
   ii. Labeling the regions and choosing material of the region.
   iii. Doping the regions and setting transverse length
   iv. Meshing of the device design and refining the mesh.
   v. Saving device drawing with extension .drw and creating .tif file of the device drawn.

2. **Device simulation:** The device simulation can be run through Device Simulation window by loading .tif file or by loading .cgns file. In Device Simulation window various simulation parameters such as electrode biasing, model selection, floating interconnections, value of boundary Z-width, and optical feature can be set. Simulations for 3-D structures codes are done through Genius Device Simulator.
3. **Extraction of results from .dat file:** After simulating the device design or the code for the device design .dat file is generated. From the spreadsheet of .dat file the desired plots can be obtained.
4. **Plot the characteristics:** The desired characteristics can be plotted by selecting the values to be plotted on respective axis for further analysis.
5. **Visualizations**: It is an important feature of this tool which gives a detailed insight to the behavior of the device. The calculations done at each step (voltage level) at all the mesh nodes are represented in the visual image form which gives the better understanding of the device. The color scheme helps in determining the variation throughout the device. Features likes electric current, electric field, potential, doping levels, holes and electron concentrations, energy levels, temperature, pressure, stress, strain etc. can be plotted in the contour. Through following images obtained from the **.vtu** files of the simulated structures, it became easy to understand the working of the device. Visualizations of 2D unstrained MOSFET structure is shown in below figures titled A, B, C and D.

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A).

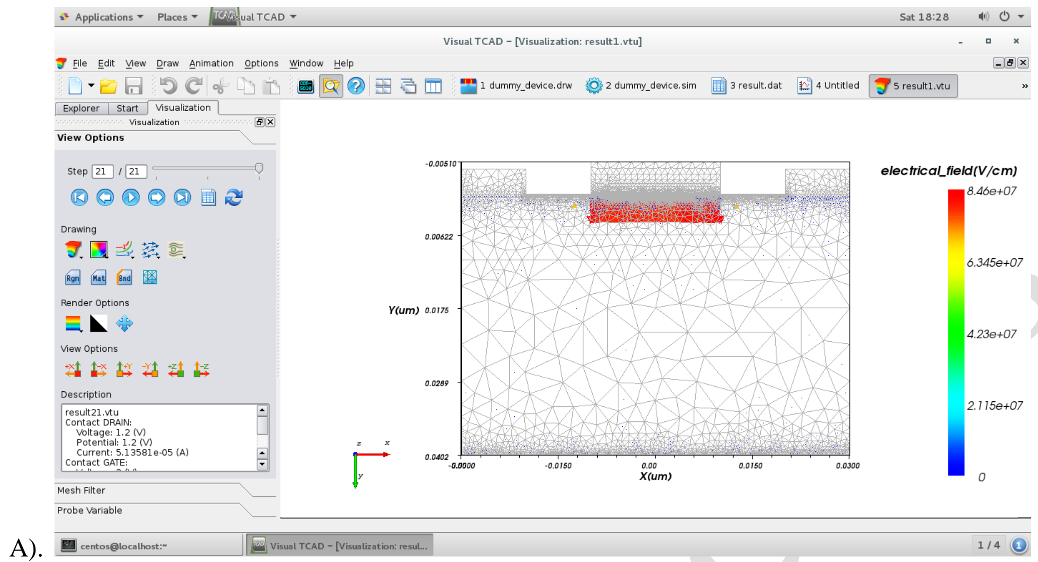


Fig. 2.2 Electrical Field in Channel

B).

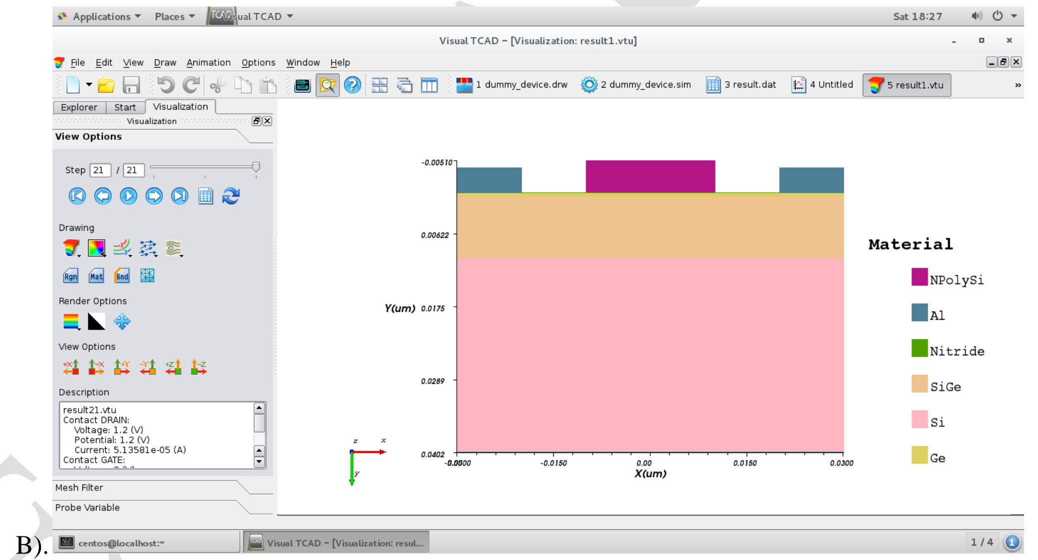
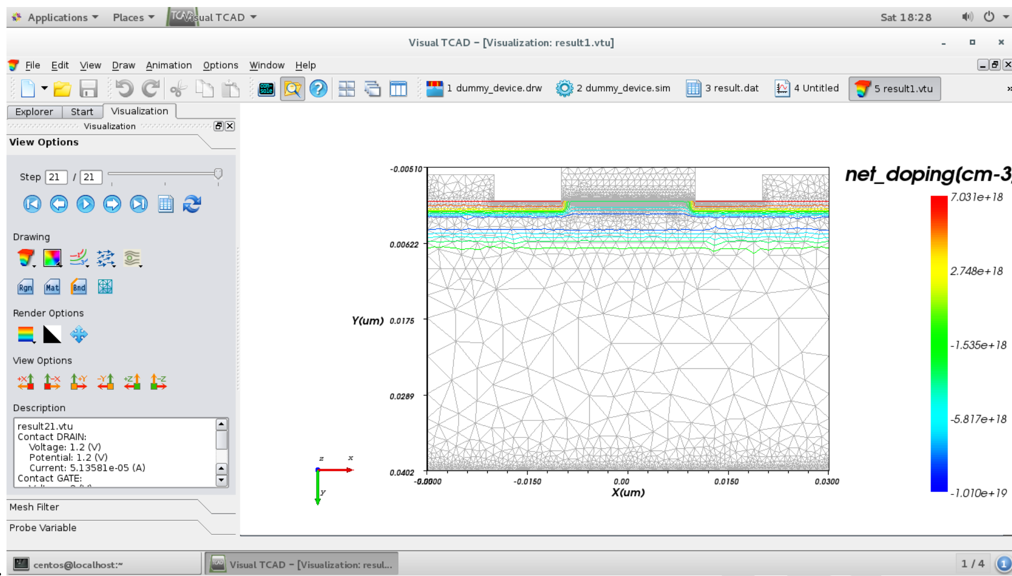
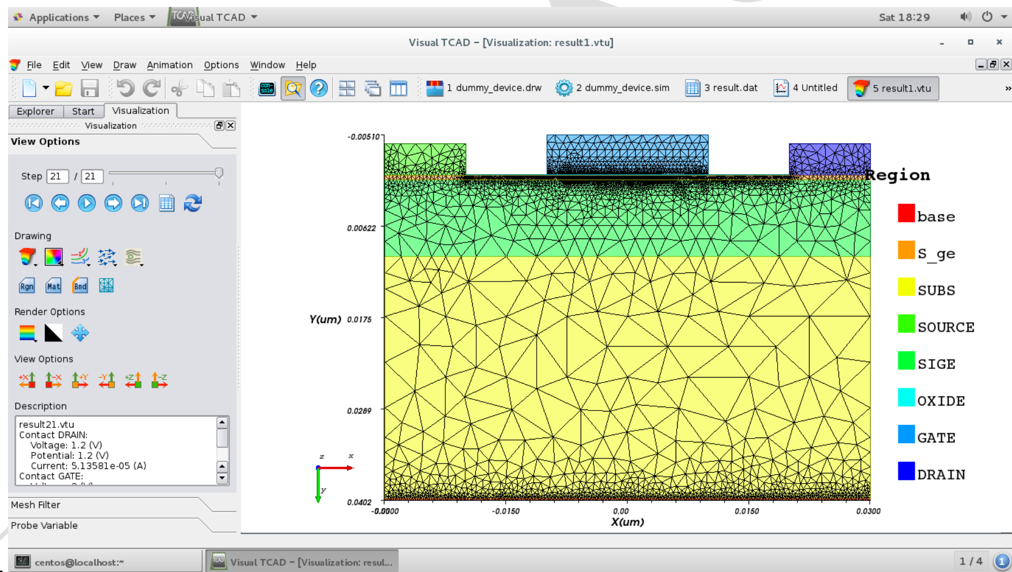


Fig. 2.3 Material Visual in different layers



C).

Fig. 2.4 Doping visual in Different Layers



D).

Fig. 2.5 Meshed visual in 2D MOSFET Structure

3. Device Structure

Strained Silicon N-MOSFET is structured in Cogenda visual TCAD. The gate length of the device is taken 20nm and device length is 30nm. The silicon substrate with width 16nm and then the SiO_2 layer of width 3nm is deposited on silicon substrate. After that the $Si_{(1-X)}Ge_{(X)}$relaxed layer is deposited on buried oxide with width of 5nm.

Linear Ge mole fraction of (10%) added in SiGe layer. Silicon channel layer of width 3nm placed on $Si_{(0.9)}$ $Ge_{(0.1)}$. All regions mentioned above are p-type doped with intrinsic boron impurity $10^{16}cm^{-3}$. Strained silicon layer is doped with 10^{17} cm^{-3}. The source and drain are highly n-doped with $10^{20}cm^{-3}$. N-Poly silicon is used as a gate material and aluminum (Al) used for body, source and drain contacts.

4. Simulation of Strain Silicon Structure

The structure is simulated in 2D TCAD simulator. The simulation profile selected with temperature 300K of different layers and interfaces. The physical equation used for calculations is Basic drift diffusion equation (DDML1), for bulk mobility calculation the Lombardi mobility model is used. The gate metal work function selected for simulation is 4.13eV. Before simulation the structure is finely meshed. After selection of the simulation profile the structure is subjected to simulation. Different simulations performed for different parameters by varying one of the parameter voltages, oxide material, Ge concentration and gate work function.

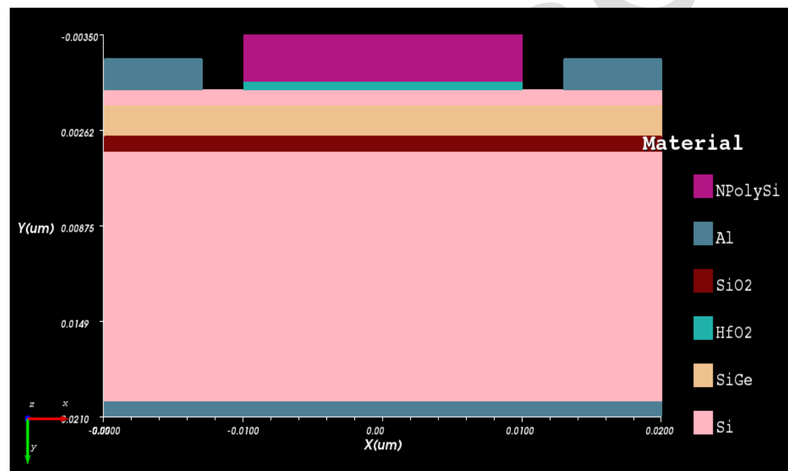


Fig.4.1 Simulated structure of single gate strained Si Si-Ge MOSFET

5. Results

Two different structure single gate silicon on insulator (SG-SOI) and single gate strained si silicon-germanium on insulator (SG-SS-SGOI) are structured with same gate length and doping concentrations simulated in TCAD 2D simulator. The comparison of both devices is done through I_d (drain current)–V_g (gate voltage) plot which shows that the strained silicon MOS have better transfer characteristics as compared to unstrained SOI structure. Due to the strain the mobility in channel increases and this increase in mobility lead to the increase in drain current (I_d). As shown in Fig.4 also the leakage current is low in SG-SS-SGOI from 2 x 10^{-5} to 6 x 10^{-7}.

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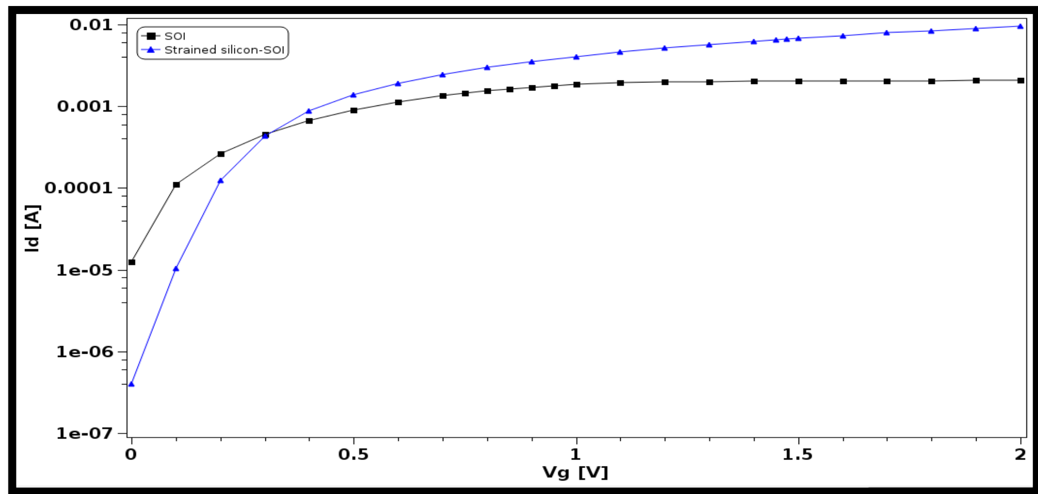

Fig. 5.1 I_d –V_g Characteristics of Strained MOSFET

The impact of strain is analyzed by increasing the Ge content in relaxed SiGe layer from 10% to 30%. The effect of strain in I_{ds}-V_{gs} curve can be seen in the fig.5. The result shows that with the increase in Ge content strain in increased, strain can be controlled with variation in Ge content [1, 3, 12] with increase in the strain the electron mobility in inversion region under the channel is peaked to 680 cm^2/V.s (fig.6) which is 80% enhancement than control SOI structure [9] and due to the impact of this high mobility the drive current also increased fig.5. Due to the integration limitations in fabrication process the Ge content is limited to maximum limit of 30% [12].

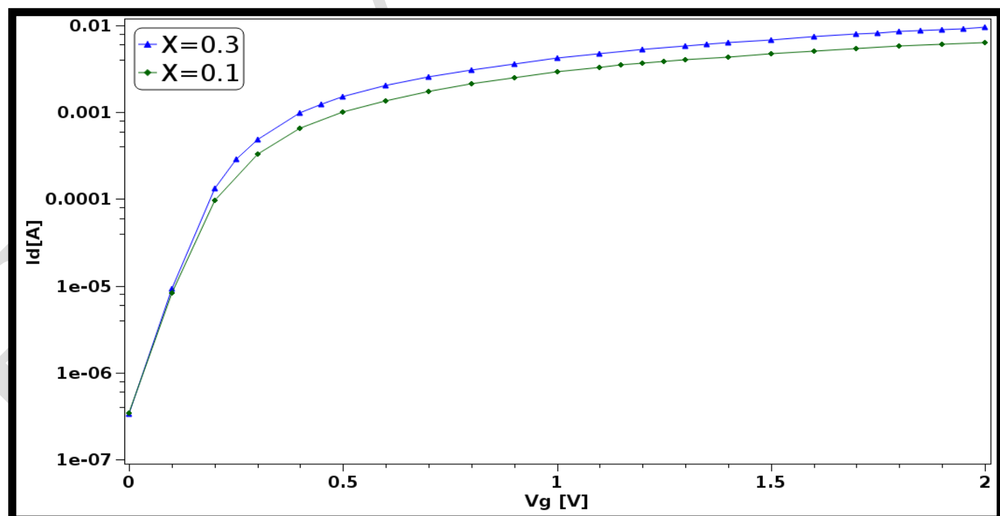

Fig.5.2 Increase in Ge mole fraction in $Si_{(1-X)}$ $Ge_{(X)}$

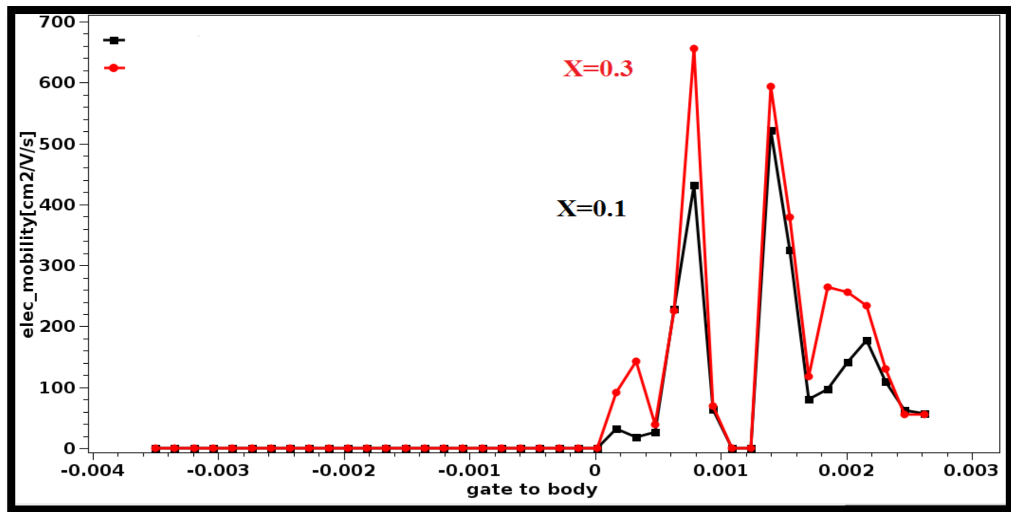

Fig.5.3 carrier mobility in SG-SS SGOI MOSFET

The impact of strain is analyzed in the channel by increasing the Ge content in $Si_{(1-X)}$ $Ge_{(X)}$ from 10% to 30%. Mobility curve in Fig.5 show the increase in carrier mobility with the increase in the Ge concentration. Also, the output drain current is increased as result of lower effective mass states due to strain. Transfer characteristics shows current ratio of the device is 10^5 which is due to leakage and scattering and is considered very low. So, to modify the performance in terms of current ratio the gate metal work function is increased as 4.5, 4.6, 4.7 and 4.8eV.It is seen that I_{off} continuously decreases with the increase in work function (Φ) as seen in fig. 7 leakage reduces while I_{on} is same and as a result the current ratio I_{on}/I_{off} is greatly increased 10^9.

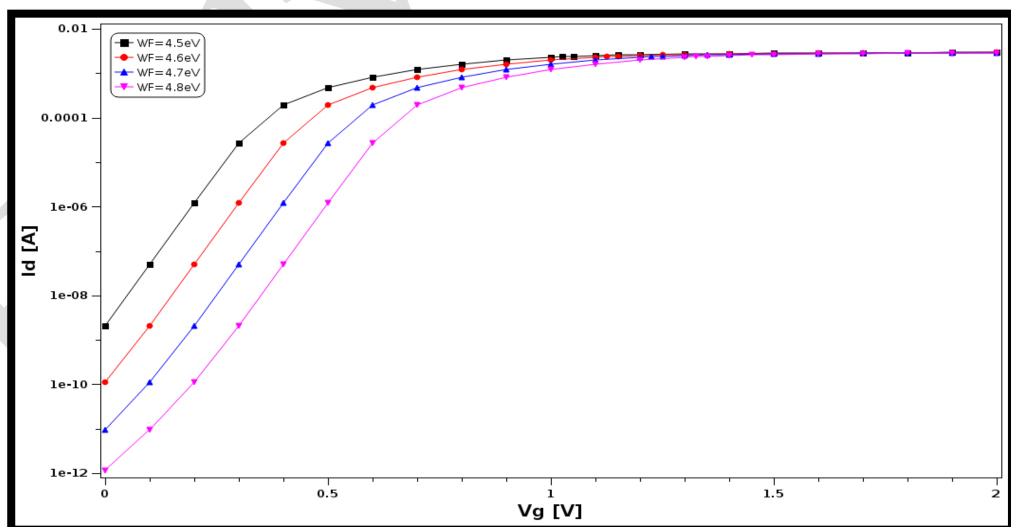

Fig.5.4 Impact of gate work function

Different gate oxide materials are also used during the simulations to analyze the impact of the oxide material on strained silicon MOSFET. High-K dielectric is one of the promising candidates to address the roadblock to the thickness of SiO2 gate oxide. But the scattering mechanisms and surface roughness at the interface of high-K gate oxide and Si degrades the surface carrier mobility. Hence for the mobility enhancement of the carriers, the conventional silicon surface can be replaced with bi-axially tensile strained silicon on relaxed Si_{1-x} Ge_x substrate which has the ability to increase both the electron and hole mobility [29]. Though the results in fig. 8 shows that three different dielectric materials (SiO_2, Oxide Stack and HfO_2) used in SG-SS-SGOI MOSFET with effective oxide thickness 0.6nm. HfO_2 with dielectric constant (ε=25) give better results. I_{on} is peaked for HfO_2 and I_{off} is lowered to 8 x 10^{-11} this affects and increases the I_{on}/I_{off} ratio.

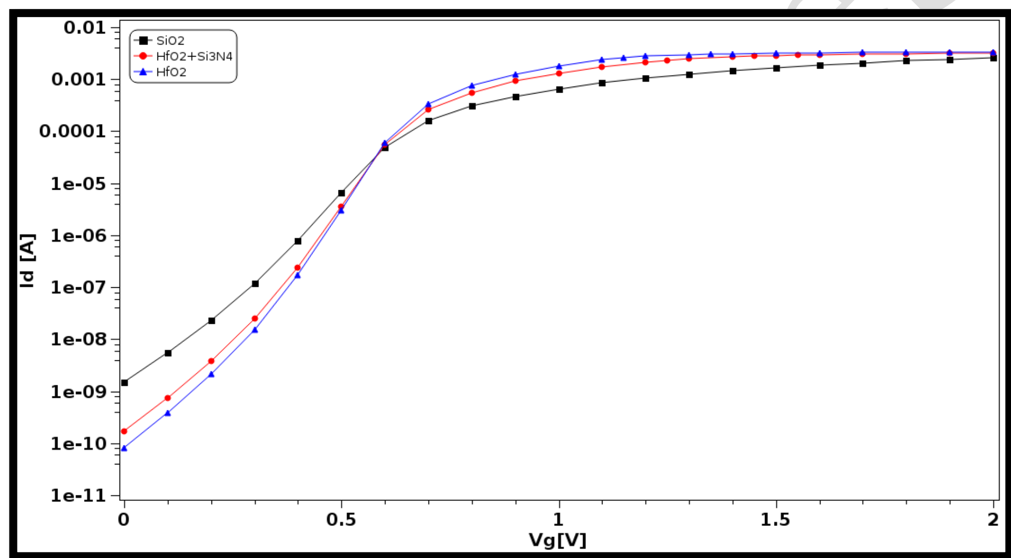

Fig.5.5 Impact of Oxide material

Sub threshold swing and DIBL effect also calculated for SG-SS-SGOI and impressive results are obtained. Sub threshold swing is negligible for devices with channel length more than 2µm but it increases sharply when channel length enters sub-micron range [18]. Strain silicon is proved to be effective in this scenario. As shown in fig.9 the DIBL effect reduces to 22mV for SG-SS-SGOI with reduction in leakage which gives that the impact of short channel effect is reduced in SG-SS-SGOI device. Sub threshold swing calculation shows that the sub threshold swing is reduced for SG-SS-SGOI to 70mV with HfO_2 as gate dielectric while sub threshold swing for SiO_2 is large fig.10.

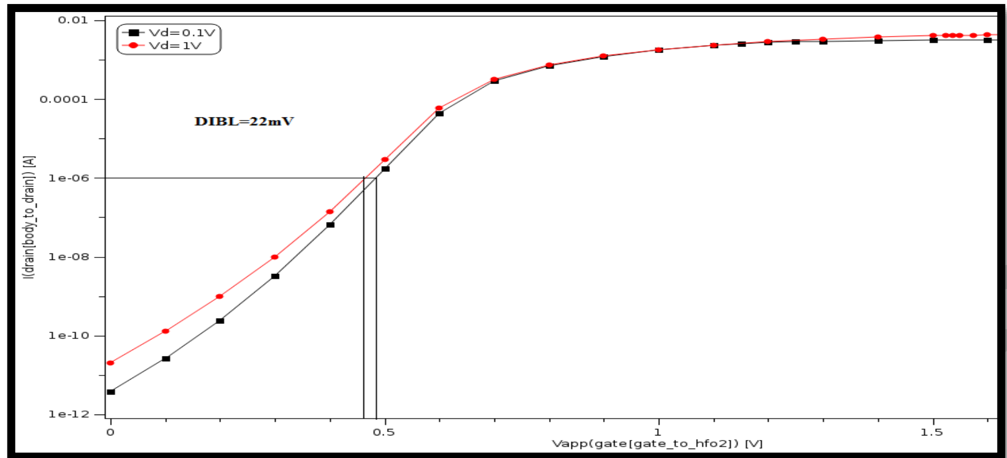

Fig.5.6 DIBL in SG-SS-SGOI

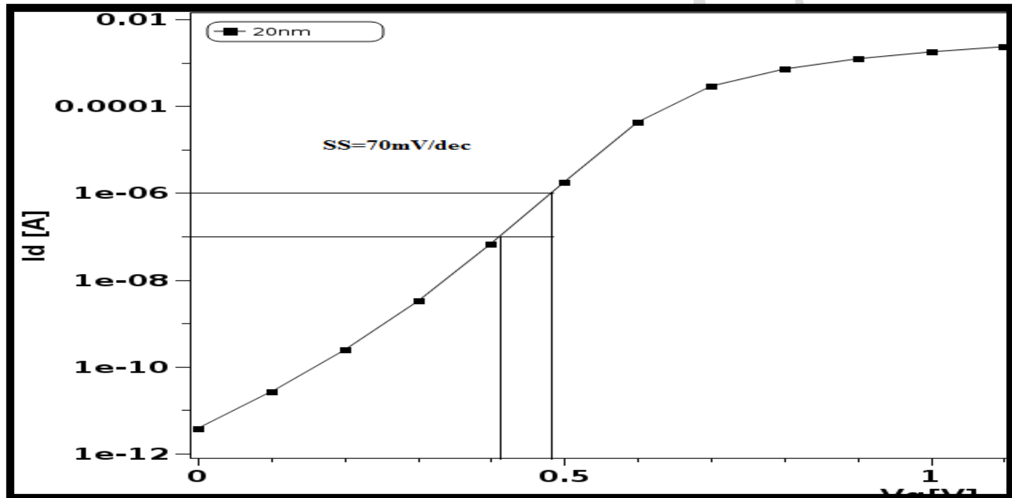

Fig.5.7 Sub threshold swing in SG-SS-SGOI

Table 1. Performance parameters

Carrier Mobility	680 cm^2/V-s
Subthreshold Swing	70mV/dec
I_{on}/I_{off}	10^9
DIBL	22mV

6. Conclusion

A 30nm SG-SS-SGOI device with gate length of 20nm have been designed and simulated in Cogenda visual TCAD. In this work the performance of SG-SS-SGOI is analyzed in Nano-scale region and improved by modifying strain, work function and gate oxide material. Earlier work in strained silicon entirely focused on enhancing the carrier mobility and so the current ratio was very low. Also, thin layer of SiO_2 was used as gate oxide in earlier works which leads to leakage in device. Previous work showed large sub threshold swing and DIBL values which is not considered as good characteristics in continuously scaled MOSFET. So, In this work high work function (Φ=4.8eV) and high dielectric gate oxide HfO_2 (ε=25) are used which shows better results in performance like carrier mobility, I_{on}/I_{off} ratio, sub threshold swing and DIBL and helped in modifying the MOSFET characteristics for its application in low power circuits.

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