A Modified Configurable Cell for Complex Function Realization in PFSCL style

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***Abstract*--This paper presents a modified configurable cell in positive feedback source coupled logic (PFSCL) style that enhances the capability of existing configurable cell in realizing complex logic functions. The existing configurable cell-based method for function realization provides efficient PFSCL designs but its benefits are overshadowed with increased number of fan-ins. The proposed modification enhances the capability of existing configurable cell in complex function realization. The usefulness of the proposal is demonstrated through realization of magnitude comparator. Three different realization of the comparator based on conventional NOR/OR gate, existing configurable cell and proposed modified configurable cell methods are introduced. SPICE simulations using TSMC CMOS 0.18 µm technology parameters are used to verify functionality and compare the performance of the circuits based on three methods. Simulation results show that modified configurable cell-based comparator's performance is superior to its counterpart, with a reduction in power consumption of 26 % & 27.5 % and an improvement in the delay by 47.17 % & 49.42 % for 4-bit and 16-bit magnitude comparators respectively, thereby establishing the concept and its usefulness.**

***Keywords*—Digital circuits, mixed-signals, PFSCL, configurable cell, magnitude comparator**

1. INTRODUCTION

With the growing need for integration and enhanced reliability, the quest of making silicon-on-chip (SoC) has received considerable attention. The high-performance digital signal processing in the chips involves the use of traditional CMOS topology based digital circuit designs due to its design ease, negligible static power and area requirement [1-5]. However, in mixed signal environments the switching noise generated by CMOS digital circuits degrades the resolution of the analog block residing on the same substrate. The problem increases manifold with rise in operating frequency in case traditional CMOS circuits are used to realize digital circuits. Researchers have worked on alternate circuit styles that work on reduced voltage swings and cancellation of the transient currents during switching events. Current mode logic (CML) satisfies both the requirements and is used for implementing low-noise digital circuits in RF applications, optical-fiber links, and high-resolution mixed-signal systems [6]. A single-ended variant of CML named as positive feedback source coupled logic (PFSCL) is especially used in design of high speed digital circuits due to inherent positive feedback mechanism [7, 8]. Logic function realization in PFSCL style can be performed by following NOR/OR gate method or by using existing configurable cell method [7-10]. A circuit design by combining the two methods has also been suggested [11]. The PFSCL circuits designed by using existing configurable cell-based method exhibits better performance than the NOR/OR gate based PFSCL design due to the lower gate count thereby improving the overall performance. However, the advantages are restricted for two/three input function. Thus, there is a need to modify the existing configurable cell structure in order to realize designs with high fan-in. So in this context the existing configurable cell is modified and a new cell structure with the aim to enhance the logic processing capabilities is proposed. The design of a 2-bit magnitude comparator is considered to highlight the benefits of using proposed configurable cell. Three realizations for the comparator based on conventional NOR/OR gate, existing and modified configurable cell methods are put forward.

The paper is organized in six sections including the introductory one. The paper briefly reviews the conventional NOR/OR gate and existing configurable cell-based methods of PFSCL circuit design in section 2. The function realization based on two methods is illustrated for a 2-bit magnitude comparator in section 3. The modified configurable

cell and its usefulness is in PFSCL circuit design is demonstrated in Section 4. Simulation section presents the results to compare performance of the PFSCL circuits based on the three methods. Conclusion of the work is presented in Section 6.

2. PFSCL STYLE

PFSCL style is often employed in digital circuit design for mixed-signal integrated systems. It is an improved version of single-ended source coupled logic style [7, 8]. A PFSCL gate has a pull down network (PDN), a current source and a load. The PDN models the functionality; current source maintains a constant bias current whereas the load performs *the current-to-voltage conversion* The gate works on the principle of current steering wherein the current is steered in different branches of the PDN depending on the inputs. A schematic of the PFSCL inverter is shown in Fig. 1(a). The transistors M1, (M2-M3), and M4 represents the current source, PDN and the load sections respectively. For high value of input A, the bias current (ISS) is steered to M2 and low output voltage is obtained at the output node Q and vice-versa.

In literature, two methods named a NOR/OR gate method and the configurable cell –based method are suggested to realize logic functions. The conventional NOR/OR method require a function to be represented in NOR/OR form which are then substituted by PFSCL NOR gate. This is due to the fact that the NOR/OR forms the basic gate in PFSCL style. The schematic of a generic k-inputs PFSCL NOR/OR gate is shown in Fig. 1(c). The k-input transistor are arranged in single level of source-coupled transistors in the PDN for NOR functionality. The same arrangement works as a OR gate if the gate output is taken from drain terminal of MF which is used to obtain different functionality [7]. The NAND functionality can be obtained by applying the inputs in the complemented form as illustrated for a 2-input PFSCL NAND gate in Fig. 1(b).

Similarly, realization of two input exclusive-OR (XOR) function requires five PFSCL NOR gates arrangement as drawn in Fig. 1(d). The cascade of PFSCL gates degrades the performance in terms of both power and delay values. An alternate method that employs configurable cell for circuit design is suggested in [9, 10]. The method reduces the gate count as well as the cascading levels The MOS schematic and symbol of configurable cell is given in Figs. 1(e) and 1(f) respectively. The cell uses two triple tail cells (TTCs) named as TTC1 (M5, M6, M8) and TTC2 (M3, M4, M7).

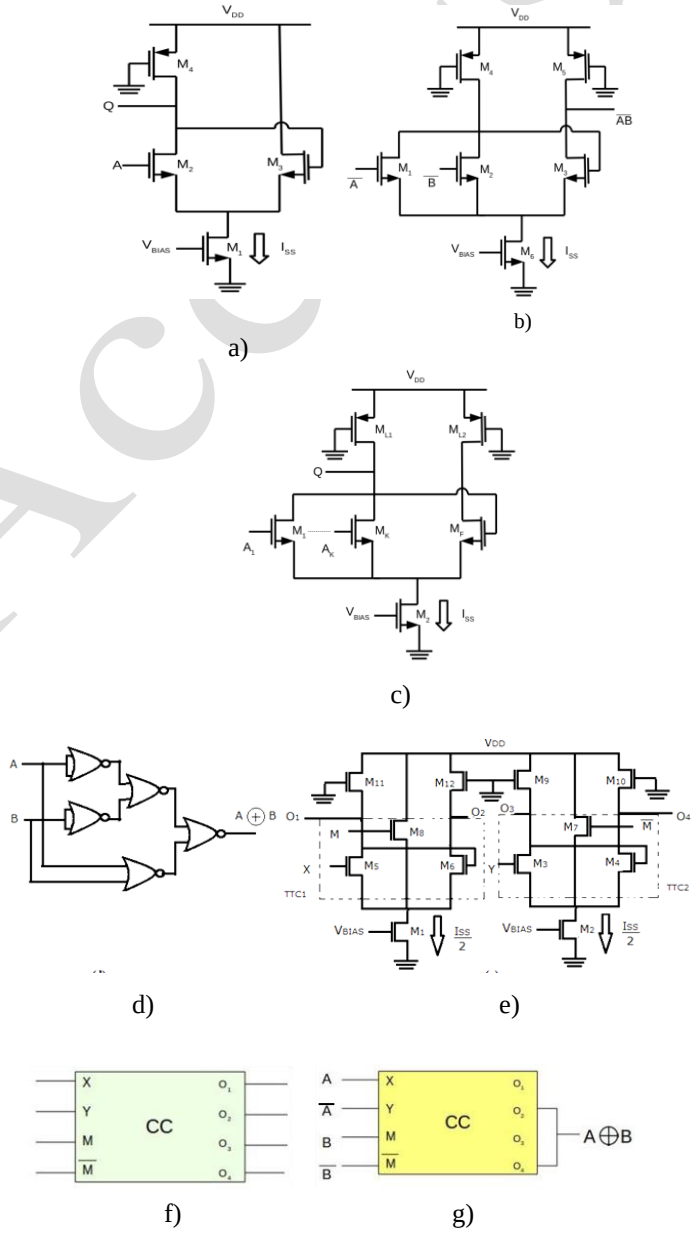


Fig. 1 (a) PFSCL Inverter (b) 2-input PFSCL NAND/AND gate (c) Generic PFSCL NOR/OR gate (d) NOR/OR based XOR gate (e) MOS schematic of configurable cell (f) Symbol of configurable cell (g) configurable cell based XOR gate realization

The inputs to the cell are applied in such a manner that at any given instance only one of the

TTC is activated and decides the output. The functionality of the cell is expressed as

$$F = k_1O_1+k_2O_2+k_3O_3+k_4O_4 \quad (1)$$

where $O_1 = M' X'$; $O_2 = M'X$; $O_3 = M Y'$; $O_4 = M Y$ and k_{1-4} are the constants. The output is computed by joining only one output node of each TTC i. e. connecting either (TTC_1: O_1 or O_2) with (TTC_2: O_3 or O_4)). A configurable cell-based two input XOR gate as shown in Fig. 1(g) wherein inputs are selected as X = Y = A, M = B, M' = B' and $k_1 = k_4 = 0$ and $k_2 = k_3 = 1$. It may be noted that XOR realization using NOR/OR method uses five PFSCL gates (Fig. 1(d)) whereas configurable cell method involves only two: one for generating B complement and one configurable cell itself. Therefore, performance improvement through configurable cell method is obvious.

3. Complex PFSCL Circuit Design

The above discussion is limited to the logic function with two input variables wherein the advantages offered by the configurable cell approach are obvious. But in some cases, the situation may differ. To illustrate this condition, the design of a 2-bit PFSCL magnitude comparator is considered. A comparator is selected as it forms an important module for applications such as searching and sorting data, image processing and 3D graphics [12-15]. Comparator is a combinational circuit that compares two numbers A and B, and determines their relative magnitude. The outcome of the comparison is specified by three functions f(A > *B*), f(A = *B*), f(A<B) that indicate whether A is greater than B (A > *B*) B), A is equal to B(A = B) or A is less than B(A < B) respectively. The simplified Boolean expressions for the three output functions of the 2-bit magnitude comparator with two numbers A (= A_1A_0) and B (= B_1B_0) are expressed as:

$$f(A>B) = A_1B_1'+ A_0B_1'B_0 + A_1A_0B0' \quad (2)$$

$$f(A<B) = A_1'B_1+ A_0'B_1B_0 + A_1'A_0'B0 \quad (3)$$

$$f(A=B) = [f(A>B)+f(A<B)]' \quad (4)$$

The NOR/OR based realization is derived by converting (2)– (4) into NOR/OR form as discussed in section 2. The gate level schematic comprising of two and three input NOR/OR gates is shown in Fig. 2. Appropriate MOS schematic of PFSCL NOR/OR gate may be used to realize comparator. This realization is now referred to a comparator realization-1 (CR-1) in the rest of the paper. It can be observed in Fig. 2 that a total of eight PFSCL NOR/OR gates for f(A>B) and f(A<B) realization while f(A=B) is obtained by performing NOR operation of f(A>B) and f(A>B). Thus, CR-1 has an overall PFSCL gate count of nine.

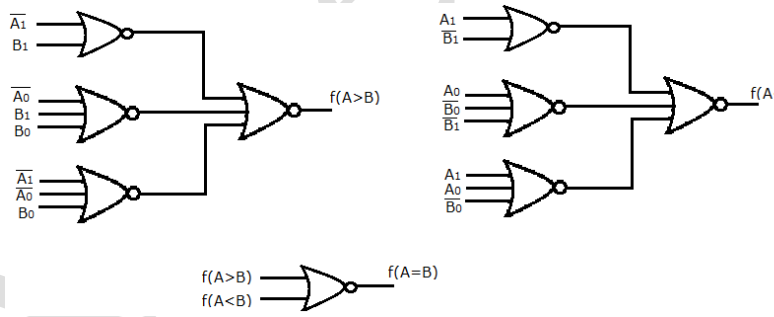


Fig. 2 Comparator Realizations-1: Conventional NOR/OR gate based magnitude comparator (CR-1)

The second realization is derived by following configurable cell-based method. The K-maps corresponding to $f(A > B)$ and $f(A < B)$ are drawn in Fig. 3 and their expressions by pairing two consecutive 1's in the map is formulated. This is done to determine the controlling variables of each TTC. The expression for the function f(A>B) is achieved as:

$$f(A>B)=A_0B_1'B_0'+A_1A_0B_0'+A_1B_1'B_0+A_1A_0'B_1' \quad (5)$$

The above equation is rewritten as:

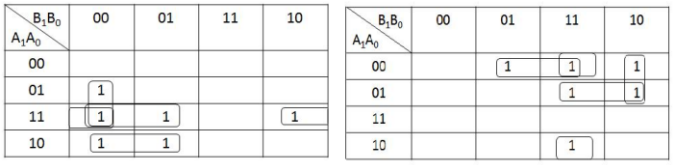
$$f(A>B) = A_0B_0'(B_1'+A_1)+A_1B_1'(B_0 + A_0') = CE'+DC' \quad (6)$$

where $C = A_0B_0'$; $E = A_1'B_1$; and $D = A_1B_1'$ is substituted. The similar approach is followed for the function f(A>B) and the resulting expression is given as:

$$f(A<B) = A_1'B_1(B_0'+A_0)+A_0'B_0(B_1 + A_1') = E F'+FD' \quad (7)$$

where F = A_0'B_0. The function f(A=B) is achieved by the same expression as written in (4).

All the intermediate terms C, C', D, E, F and F' are generated by configuring configurable cell as a two input AND/OR gate. The complete block diagram for the proposed configurable cell-based comparator realization (CR-2) is shown in Fig. 4. It can be observed that the CR-2 uses ten PFSCL gates as against nine in CR-1. Thus, there is a need to optimize the structure of the existing configurable cell. Next section addresses this issue and presents a modified configurable cell.



a) b)

Fig. 3 . K-Maps a) f(A>B) b) f(A<B)

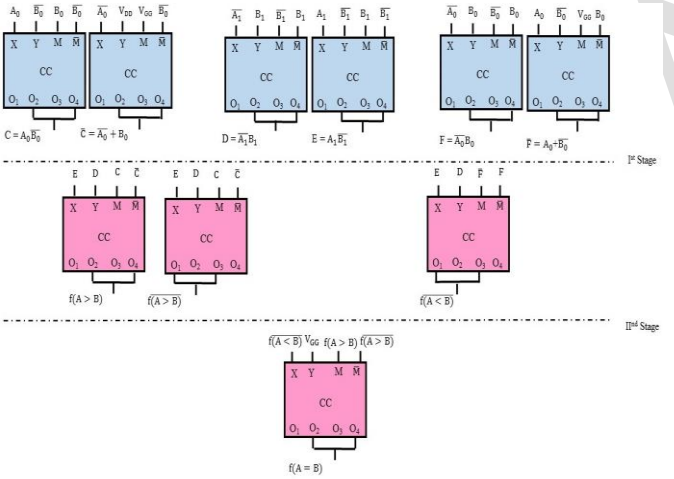


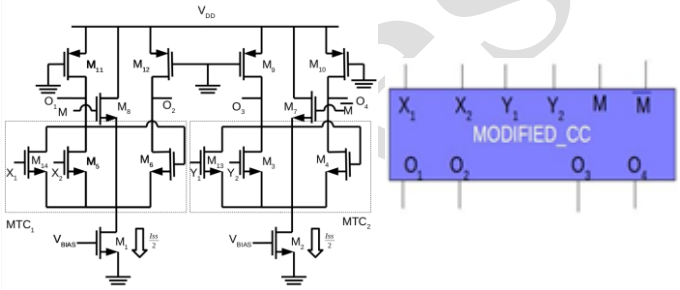
Fig. 4. Comparator Realization-2: Configurable cell based proposed magnitude comparator realization (CR-2)

4. Proposed Modified Configurable Cell

The capability of the existing configurable cell is enhanced by transforming the concept of tripe-tail to multi-tail. To achieve this, an additional transistor is attached in each TTC of the existing configurable cell (Fig. 1(e)). The circuit can now be viewed as two multi-tail cells (MTC) consisting of transistors (MTC1: M5, M14, M6, M8,) and (MTC2: M3, M13, M4, M7,) with input signal M and $\overline{M}$ used for activation/deactivation purpose. The complete MOS schematic of the modified configurable cell (MODIFIED_CC) along with its symbol is shown in Fig. 5. The additional transistors now provide the capability of realizing NOR/OR functions by the cell. The output of MODIFIED_CC can be expressed as:

$$F = K_1O_{m1} + K_2O_{m2} + K_3O_{m3} + K_4O_{m4} \quad (8)$$

Where O_{m1}= M'(X_1+X_2)'; O_{m2} =M'(X_1+X_2); O_{m3}=M(Y_1+Y_2)'; O_{m4}=M(Y1+Y2)



a) b)

Fig. 5. Proposed modified configurable cell a) MOS schematic b) Symbol

The conditions on k1-4 remains the same as discussed in section 2. The modified cell can be configured for various functionalities by appropriate selection of input variables and k1-4. It may further be noted that the number of parallel transistors in outer branch can be increased further to enhance the functionality. Based on this concept, we propose a third realization, modified cell based magnitude comparator (CR-3) and is drawn in Fig. 6.

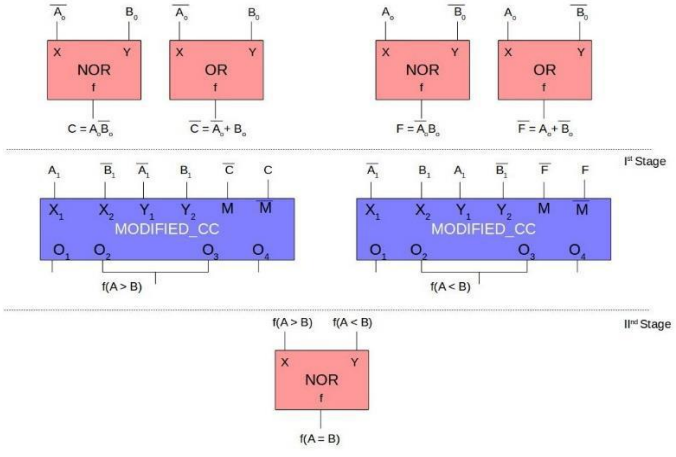


Fig. 6 Comparator Realization-3: Proposed Modified Configurable Cell based magnitude comparator (CR-3)

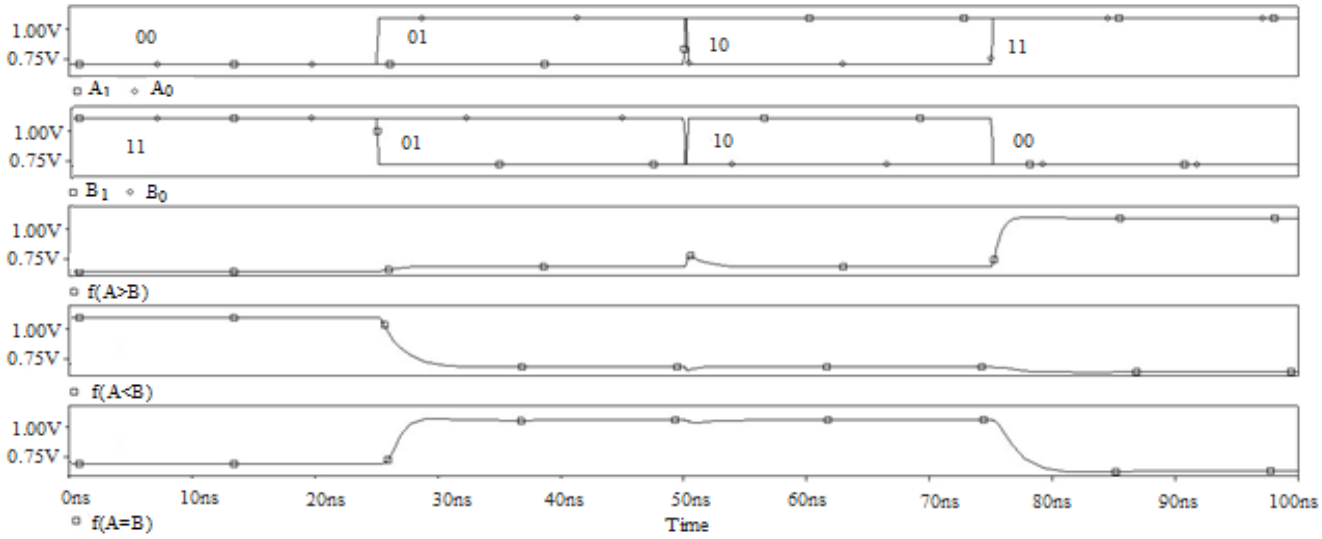


Fig. 7 Simulation waveform of 2-bit PFSCL magnitude comparator using proposed modified configurable cell

In order to understand the design, the equations corresponding to $f(A > B)$ (7) and $f(A < B)$ (9) are revisited. The functions (C and C') and (F and F') are generated by PFSCL NOR/OR gates and are connected to middle transistors of the MODIFIED_CCs for proper activation/deactivation. The MODIFIED_CCs provide functions f(A>B) and f(A<B). The third stage uses a PFSCL NOR gate to compute the result for f(A=B) as given by (4). The overall gate count in CR-3 is seven in contrast to nine and ten in CR-1and CR- 2 respectively.

5. Simulation Results

In this section, the functionality of the proposed modified configurable cell is verified and then its effectiveness in PFSCL circuits realization is evaluated. The three realization of the magnitude comparator are simulated and their performance is compared. The impact of process variation is also studied. The proposed 2-bit magnitude comparator realization is extended to design higher order magnitude comparator. All the simulations are carried out by using TSMC 0.18 µm CMOS technology parameters and a power supply of 1.1 V. A bias current of 100 µA and voltage swing of 400 mV is maintained for all gates. It is also assumed that complements of the inputs are also available.

5.1 Functional Verification

The functionality of the proposed modified reconfigurable cell is verified through the simulation of 2-bit PFSCL magnitude comparator (CR-3)(Fig. 6). The waveforms of the magnitude comparator are shown in Fig. 7. It can be observed that the comparator outputs are in accordance with the inputs. Thus, ensuring the correct operation of the cell.

5.2 Performance Comparison with the Existing Methods

Performance The performance of the proposed magnitude comparator realization is compared in terms of gate count, transistor count, delay, power consumption followed by the impact of parameter variations. The findings are comprehended in Tables 1 and 2. The following observations can be made from the results

- The overall gate count in CR-2 is maximum which results in degraded performance parameters in comparison to CR-1 and CR-3. This clearly dictates the need for modification in the existing realization of configurable cell.
- As the power consumption in PFSCL gates is computed as the product of the gate count, power supply and bias current values, CR-3 based comparator design exhibits least power consumption Additionally, CR-3 based design has reduced delay values due to reduced

capacitance at output node in configurable cell than CR-1.

- The results of process variation on comparator design through the three methods shows that there is a maximum variation of 1.85, 2.01 and 1.71 between the best and the worst cases of CR-1, CR-2 and CR-3 realizations respectively.

On the basis of the above analysis, it is clear that the proposed modification in the configurable cell has regain its benefits leading to efficient PFSCL system realizations.

TABLE I. SUMMARY OF THE SIMULATION RESULTS OF THE PROPOSED MAGNITUDE COMPARATOR

Circuit / Parameter	CR-1	CR-2	CR-3
Gate count	9	10	7
Transistor Count	49	120	53
Delay (ns)	3.241	3.438	2.086
Power Consumption(µW)	990	1100	770

TABLE II. SUMMARY OF THE SIMULATION RESULTS OF THE PROPOSED MAGNITUDE COMPARATOR

NMOS / PMOS / Parameter	T T	F F	S S	F S	S F
CR-1					
Delay(ns)	3.241	2.301	3.855	2.522	3.582
Power Consumption(µW)	990	1452	781	1256	854
CR-2					
Delay(ns)	3.438	2.590	4.584	2.702	3.923
Power Consumption(µW)	1100	1641	815	1548	879
CR-3					
Delay(ns)	2.071	1.788	2.367	1.841	2.223
Power Consumption(µW)	770	1129	658	807	728

C. Higher Order Comparators

The 2-bit magnitude comparator realization (CR1-3) are extended to realize high order comparators such as 4-bit, 16-bit. Three 2-bit comparators are used to design 4-bit comparators whereas five 4-bit comparators are connected for 16-bit comparator design. Their design is represented in the block diagram shown in Fig. 8.

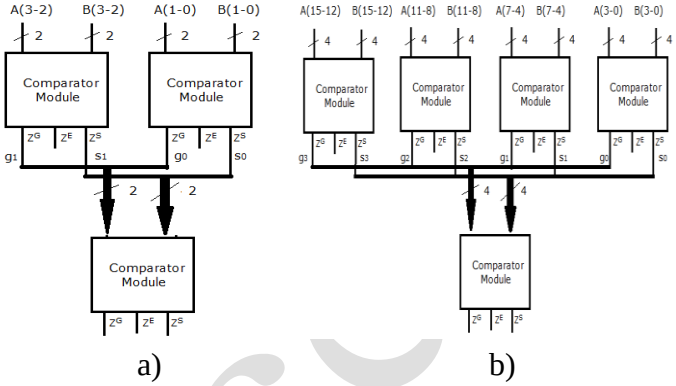


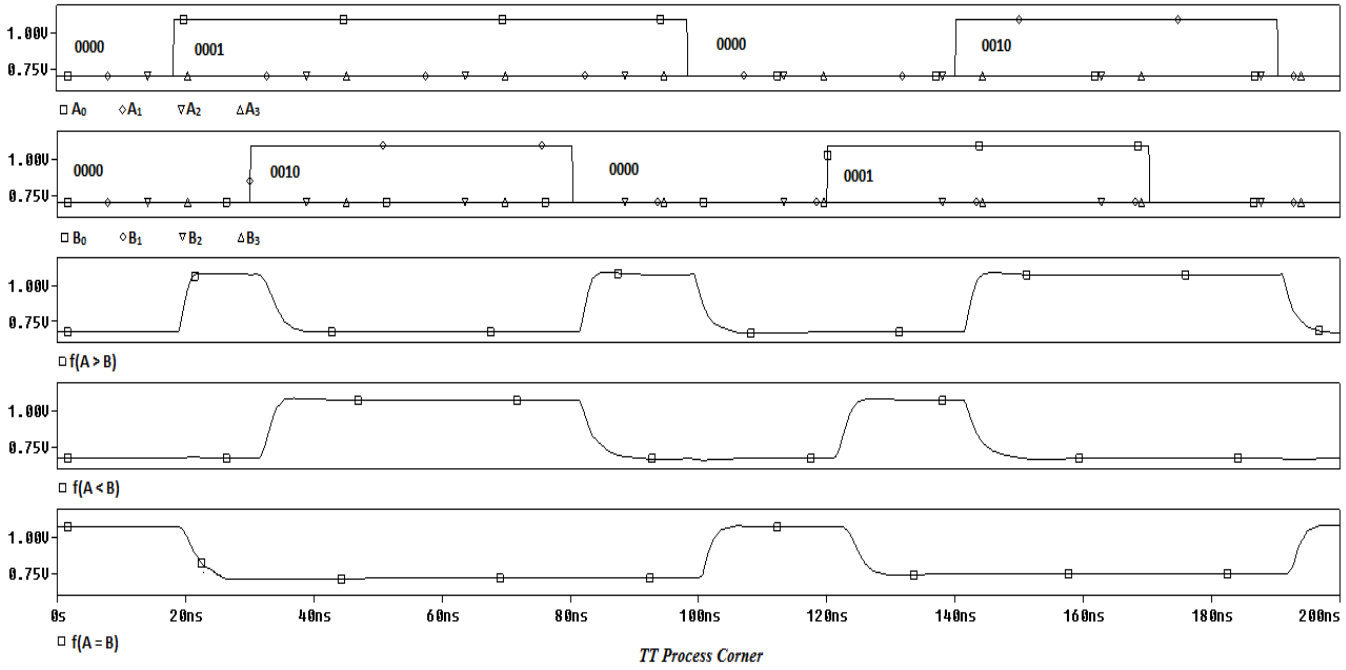
Fig. 8 Design of (a) 16-bit comparator (b) 4-bit comparator employing a tree network

The comparators are realized by all three methods and their waveforms are shown in Fig. 9. A performance summary is presented in Table 3.

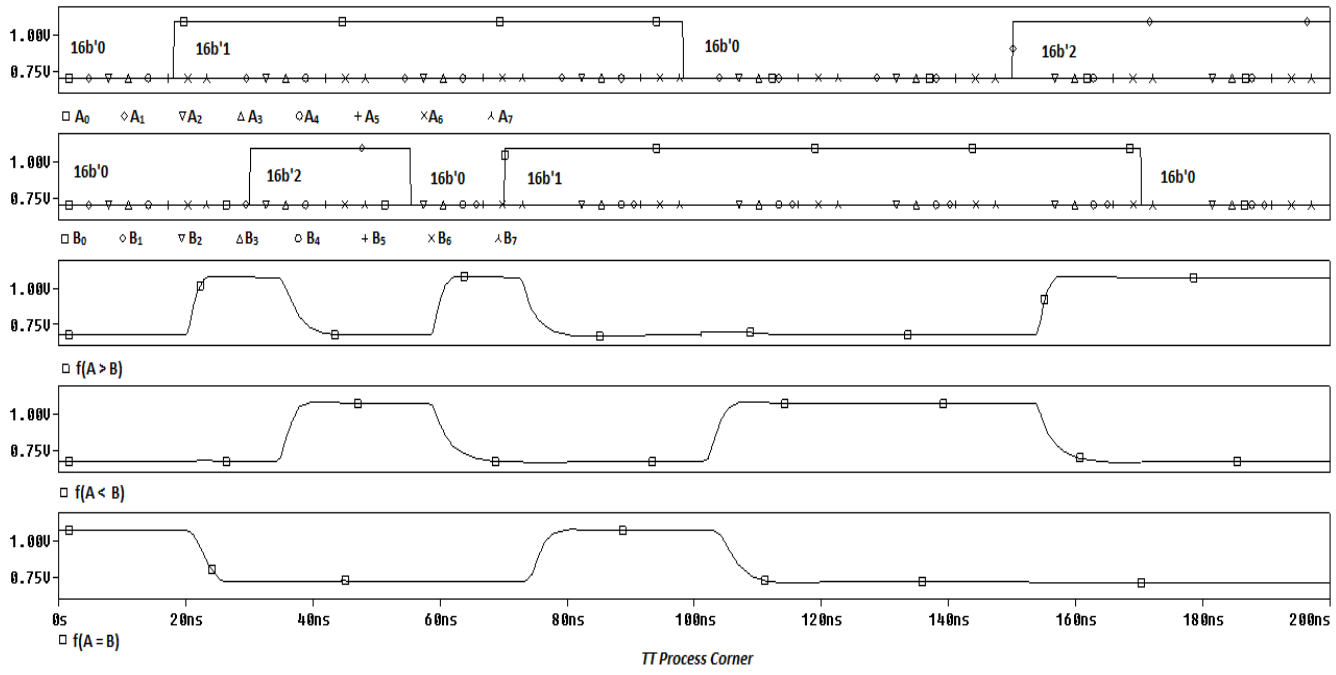
The 4-bit comparator based on CR-3 offers a maximum saving of 30 % & 52 % in the power consumption and delay values with respect to the other two comparator designs.Similar improvements are observed for the 16-bit PFSCL magnitude comparator based on CR-3.

6. CONCLUSION

A modified PFSCL configurable cell is proposed in this paper which is suitable for complex function realization. A magnitude comparator has been chosen to elaborate the concept and this design is compared with circuit realizations based on PFSCL NOR/OR gates and existing configurable cell-based gates. It was found that the existing configurable cell-based design uses larger number of gates for increased number of inputs than modified configurable cell-based design proposed in the paper. SPICE simulations using TSMC 0.18 µm CMOS technology parameters are performed for functional verification and performance comparison. The results show that the circuit realization with modified configurable cell reduces the gate count and consumes lowest power. The feasibility of the proposed architectures in high



a)



b)

Fig. 9 Simulation waveforms of Arch-3 based magnitude comparator a) 4-bit b)16-bit

order magnitude comparator design is demonstrated wherein the simulation results conforms the earlier results. Thus, the modified configurable cell provides an efficient design option to designers.

TABLE III. SUMMARY OF PERFORMANCE

Circuit Parameter	CR-1	CR-2	CR-3
4-bit PFSCL magnitude comparator			
Gate count	27	30	21
Transistor Count	147	360	159
Delay (ns)	7.052	8.46	4.064
Power Consumption(µW)	2970	3300	2310
16-bit PFSCL magnitude comparator			
Gate count	135	150	105
Transistor Count	735	1800	795
Delay (ns)	16.367	20.31	9.168
Power Consumption(µW)	14850	16500	11550

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