A Review Paper on Low Power Address Generators for Memory Testing

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***Abstract*— In VLSI Industry Power and Overall delay were the major factors in the design concern. In the manufacturing of Integrated Chips enormous of failures will occur due to the production error and design error. In System on Chip (SOC), memory is more likely to be affected by manufacturing faults. Built-in-self-test is the efficient method for testing of embedded memories as it saves testing time. Major testing element is a linear feedback shift register (LFSR) which act as an address generator. Switching activity in the LFSR is the main cause of the increase in power during the test. So, in this paper, there is a review of implementations of different types of low power address generators with respect to the switching activity.**

***Keywords*— LFSR, BIST, SOC, VLSI, TPG**

1. INTRODUCTION

In VLSI, the cost, performance, area, testing, and reliability are the most important parameters to be considered at the time of designing. The demand for embedded system portable computing devices and communication system is increasing day by day. The main important challenge is testing of System-on-Chip. The important testing challenge is memory testing. The testing of embedded memory has an important role in the process of testing of System-on-Chip (SOC) for detecting faults and improving overall yield and quality. The modern memory designs should have higher storage capacity with the lower area and should have the fastest access speed. The requirement for storing the data is very important these days, so there is a strong demand for RAM with lower power consumption with higher performance. In the near future, 90% of space will be occupied by memory in SOC, and due to very large scale integration and complex structures, the memory is affected by defects. Therefore the important testing challenge is memory testing. In VLSI circuits, the power requirement in test mode is more as compared to normal mode. Memory testing again dissipates more power. Generally, a system consumes more power in test mode than in normal mode [5].

Modern memory designs aim at high capacity at lower area and fast access speed. This leads to a situation where we have very less charge stored per memory cell (because of low capacitance), and cells are extremely close to each other.

Therefore multiple faults will be present in any memory IC's. Therefore the yield of a memory chip is 0%. With reference to the growing complexity of VLSI designs, require testing issues to be considered early in the design process so that the design can be modified to simplify the testing process. In the manufacturing department, these fault models are grouped into different clusters depending upon the fault type. The fault present in ICs was classified into three different types, namely Permanent Fault, Temporary Fault, and Delay Fault. The permanent Fault will affect for a Long time in the IC, and we can't eliminate this Fault easily unless recreation of ICs.and temporary fault will appear and disappear at a short period of time due to the time-varying IC property. Finally, the delay Fault depends upon the operating speed of the ICs. Testing and debugging of the Circuits was a more important and complex task in the very large scale integration industry. A lot of methodologies practically used to test the circuits at the manufacturing stages. The two

major schemes for testing were followed are DFT (Design for Test), ATPG (Automatic Test Pattern Generation). DFT scheme having more advantages compare to the ATPG due to its fast processing rate, testability rate, and high complexity. In recent times VLSI semiconductor industry affects a lot of advancement Page Layout, which leads to the hundreds to thousand number of in build transistor count. It leads to increased complexity in the testing schemes. In VLSI Industry Power and Overall delay were the major factors in the design concern. In recent years emergence in portable mobile devices leads to the reduction in the power dissipation not only the circuit power also in testing power.

During Testing Process, we have to optimize the testing speed and testing power. If these testing vectors are not optimized for the power means these CUT (Circuits under Test) will dissipate the double the amount of power when compared to the normal operating conditions [6]. While researching this reason, we found that these testing circuits need a large number of testing vectors, which leads to high power dissipation. These testing vectors produced by the test circuit were independent of the CUT and its leads to the higher clocking period, which also affects higher power dissipation. As a result, we have to optimize these testing parameters. These parameters include testing speed, power dissipation while Testing, Fault Coverage Rate, and Overall Testing Circuit Area. There is no definite relationship between successive address patterns generated by a linear feedback shift register for built-in-self-test. Due to the lack of correlation between the addresses generated by the LFSR, the switching activity will rise at the time of testing the memory elements. This switching activity is related to power dissipation in CMOS circuits. It is directly proportional to switching activity. By reducing switching activity, power consumption can be reduced. Reduction in these factors like Testing Power, Testing Time, Fault Coverage, and Overall Area was complex for design Industry. So that many researchers have focused improvement in the existing LFSR to reduce the Overall Testing Delay and Testing Power.

Built-in-self-test emerged as a promising solution for testing memory. It has the capability of the circuit (chip, board, or system) to test itself.BIST techniques can be classified into two categories, namely on-line BIST and off-line BIST. In on-line BIST, testing occurs during normal functional operating conditions, i.e., circuit under test (CUT) is not placed into a test mode. There are two types of on-line BIST. In concurrent on-line BIST testing occurs simultaneously with the normal functional operation. This form of testing usually accomplished using coding techniques or duplication. In non concurrent BIST, testing is carried out while a system is in idle state. The test process can be interrupted at any time so that normal operation can resume.

Off-line BIST deals with testing a system when it is not carrying out its normal functions. Systems, boards, and chips can be tested in this mode. Off-line testing does not detect errors in real-time. There are two types of off-line BIST. A functional off-line BIST deal with the execution of a test based on a functional description of the CUT and often employs a functional or high-level fault model. Structural off-line BIST deals with the execution of the test based on the structure of the CUT. Fault coverage is based on detecting structural faults. Usually, tests are generated, and responses are compressed are using some form of an LFSR.

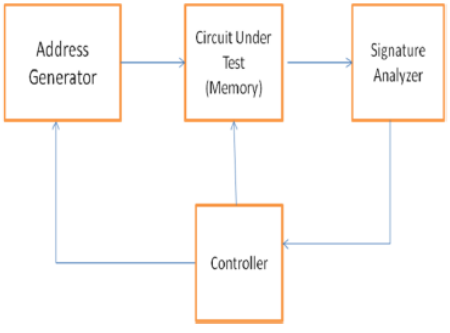

Fig.1: Architecture of Built-in-self-test

The paper is related to the reduction of switching activities in the circuits. To achieve superior power reduction, the major clock using unit was LFSR. Here LFSR used for the purpose of generating the random address for the memory under test. So the objective of this paper is to design and implement an improvised clocking scheme for the LFSR circuit and have to reduce the overall power consumption.

Single Event Upset (SEU) is the soft error in the RAM. In SEU a single high energy particle strikes a critical node and leave behind an ionized track. It will arise due to the unmoral radiation on the Memory area on the RAM There is a change of "0" to "1" and "1" to "0". Usually, there are no testing methods available for the type of problems. This will leads to a higher fault possibility in the RAM circuits [2].

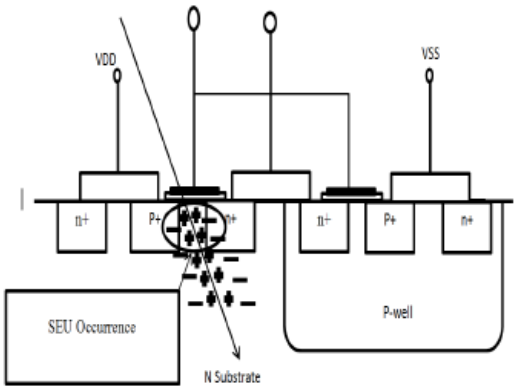

Fig. 2: SEU in CMOS memory cell

2. MEMORY FAULTS

2.1 Stuck-at-fault

Stuck-at-fault in memory is the fault in which the logic value of a cell either stuck to "0" or stuck to "1".This is the major fault found in memory circuits.

2.2 Transition fault

In transition fault, the cell can not be able to make a transition from either (0 to 1) or from (1 to 0). There are two transition faults up and down the fault.

2.3 Coupling Faults

This fault arises due to the coupling between the cells.

2.4 Bridging fault

A bridging fault arises due to a short circuit between two or more cells. Only two cells are involved in a bridging fault.

3. POWER ANALYSIS

In any electronic devices, there is a conversion of electrical energy to heat called as power. Equation (1) represents the power dissipation in electric circuits

$$P=V.I \quad (1)$$

Where:

V = Voltage , I = Current , P = Power

CMOS technology is used for low power designs. Today's most of the designs are based on CMOS technology, so it is important to understand the sources of power dissipation in memory devices. Sources of power consumption in CMOS circuits are categorized into three types: Static power dissipation and dynamic power dissipation Equation (2) shows the relationship between these power processes.

$$P_{average} = P_{static} + P_{dynamic} + P_{short\ circuit} \quad (2)$$

Memories have very low static power dissipation, and most of the energy in them is used to charge and discharge the cell load capacitances. Dynamic power is the main source of power dissipation. Therefore the static and short circuit power dissipation can be ignored. Therefore, dynamic power is the principal source of power dissipation in CMOS devices [6].

3.1 Static Power Dissipation

Static power dissipation occurs when the logic-gate output is stable; thus, it is frequency independent [4].

$$P_{static} = V_{DD}. I_{leakage} \quad (3)$$

Short-Circuit Power Dissipation

This type of power dissipation occurs when there is a flow of current from power supply to the ground during the state changes taking place. The value of short-circuit dissipation depends on the amount of short-circuit current flowing to GND [4].

$$P_{short\ circuit} = V_{DD}. I_{short\ circuit} \quad (4)$$

3.2 Dynamic Power Dissipation

There are two types of power dissipation in CMOS devices dynamic power and static power. Dynamic power accounts for 90 % of overall power consumption. Therefore it is the dominant source of power dissipation. Dynamic power occurs during the state changes of logic gates, and therefore, this type of power dissipation is dependent on frequency. Therefore dynamic power is the average power.

4. LITERATURE SURVEY

4.1 Address Generators

LP-TPG

Srilatha & Rakesh designed an address generator for built-in-self-test structures used for testing memory elements. Address generator consists of a basic element of BIST which is linear feedback shift register, and it also consists of a counter and a grey code generator which are exclusively ORed with the seed generated by low power LFSR[4]. Initially, the counter is initialized with zeros, which generates 2n test patterns in sequence. The n-bit counter and grey code generator are controlled by a common clock signal. The output of the m-bit counter is act as input to the NOR gate and gray code generator structure. When all the bits of counter output, then the output of NOR gate is one. For the generation of next seed, the NOR gate output should be one so that the clock signal is applied to activate the LP-LFSR. The seed generated from LP-LFSR is Exclusively ORed with the data generated from the grey code generator. The addresses generated from the exclusive OR array are the final output patterns. This method significantly reduces the power consumption during testing mode with the minimum number of switching activities using LP-LFSR [4].

DS-LFSR

Wang and Sandeep K.Gupta proposed an address generator for built-in-self-test which consists of dual speed LFSR (DS-LFSR) that is slow LFSR and a normal speed LFSR. The slow LFSR has been applied with slow clock and normal speed LFSR has been applied with a normal clock. Due to the use of DS-LFSR, the frequency of switching activities by the slow LFSR reduces, which significantly reduces the power dissipation. There is 17% to 70% reduction in the number of load capacitance weighted transitions with no loss of fault coverage and very slight area overhead [3].

BS-LFSR

Abbu Issa & Steven present a novel low transition linear feedback shift register (LFSR) that is based on the output sequence of a conventional LFSR. Bit-swapping LFSR composed [1] of an LFSR and a 2x1 multiplexer. In this address generator, there is an exchange of neighboring bits in LFSR structure. The last bit is the control bit, which is the selection line for the swapping process. If the last bit id 0, then swapping is performed, otherwise nothing will change. It was proved that the BS-LFSR reduces the switching activity in the inputs of the Circuit under Testing about 25% [1].

Table 1: Comparison of switching activities of different address generators [5]

Address Bus Length (bits)	Testing Time (ns)	LP-LFSR (SA)	BS-LFSR (SA)	DS-LFSR (SA)
5	128	85	69	70
10	4096	5130	4106	2904
25	134217688	419430211	318767107	218202082

Table 1 shows the comparison of three address generators in terms of address bus length and testing time using Built-in-self-test. In every address generators, LFSR is used in different ways.

As there is a low correlation between the addresses generated by LFSR, the switching activities are increased. So there is large power dissipation. The main advantage of using the LFSR as an address generator is the low overhead in the hardware area. In bit swap (BS) LFSR, the switching activity is reduced due to the swapping process as compared to LP_LFSR . There is no change in the switching activity if we change the seed. From the table, if we compare the frequency of transition between DS-LFSR and BS-LFSR, DS-LFSR has better in reducing the switching activity than the BS-LFSR since the frequency of transitions is reduced. The DS-LFSR reduces power consumption very effectively.

The bipartite LFSR is also efficient in reducing the switching activity, but using this address generator may lead to redundancy in the sequence of addresses generated, and this will reduce the fault coverage achieved within the same testing time [5].

5. CONCLUSION

After the analysis of all types of address generators, it is observed that bipartite LFSR will need more testing time as compared to DS-LFSR and LP-LFSR. Bipartite LFSR reduces instantaneous power more than average power. If we use DS-LFSR with BS-LFSR for its slow and normal generators reduces switching activity significantly. The fault coverage will also be more. It could be found from the results that using this combination has the least switching activity in the address decoder.

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