A 2-bit Current-mode ADC based on the Flipped Voltage Follower Technique

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***Abstract*— This paper presents a novel 2-bit current-mode Analog to Digital Converter (ADC), expandable upto n-bits. It utilizes a voltage follower cell termed as flipped voltage follower (FVF) in its input stage, followed by an FVF based current comparator design. It provides a fairly good response for supply voltages as low as 1.2V, thereby ensuring low power consumption. The functionality of the proposed structure is verified using SPICE simulations using 0.18 µm TSMC CMOS technology parameters.**

***Keywords*— Analog-to-digital converters, Current-mode, Flipped Voltage Follower, Current sensor, Current Comparator, Encoder**

1. INTRODUCTION

Digital signal processing is fast finding application in the diverse real time application fields, right from communication to multimedia to control systems, power electronics and so on. All these applications require digital signals for processing and application. However, all real time signals are largely analog in nature. Thus, there is always a need for an interface that can convert the real time analog signals into their digital counterparts for processing using digital signal processing based systems. This interface is provided by a medium called ADC. An ADC converts an analog signal into its digital equivalent form.

There are numerous ADCs classified based on their features and specifications. A class of ADCs based on the type of analog input signal they process, can be identified as a voltage mode ADCs and a current-mode ADCs. Current-mode ADCs offer better performance than the former, in terms of lower circuit capacitances, faster switching speeds, reduced voltage swing etc.

The current-mode ADC operation essentially consists of comparing an input current value to a reference current value by the means of a circuit called a current comparator. Thereupon, this comparison output is encoded into the corresponding digital code using a suitably designed encoder for the purpose. Choice of a suitable current comparator for implementing an ADC is the most critical aspect. While designing or selecting a current comparator, important parameters that need to be taken care of are lower input impedance and higher speed. Numerous current comparator architectures have been reported in literature over the past few decades [1-9]. Their limitations include high power supply, larger propagation delay, complex circuitry and non-achievability of rail to rail output swing.

As the trend towards large mixed signal ASICs is fast growing, for an ADC to be useful within a fully integrated VLSI system, it is imperative that the ADC should be compatible with the available digital technology, be smaller in size and should consume less power while still maintaining a high sampling rate [10-11]. High sampling rate requirement can be met with by reducing the settling time required taken by the voltage over circuit capacitances and the associated parasitic capacitances [12]. To accomplish this goal, current signals in place of voltage, can be used. This allows for the

exploitation of the nonlinear I- V relationship of most active devices in order to reduce the voltage swing for a given signal range. Thus this methodology is receiving increasing interest [13-14].

Further, in order to address the low power consumption parameter, various techniques such as folding, triode-mode and sub-threshold operation of MOS transistors, floating-gate techniques, and current-mode processing have been proposed in literature to reduce supply voltage requirements in analog and mixed-signals circuits [15-19].

As an effort to overcome the above mentioned tribulations, in this paper, a low voltage high performance current-mode ADC is elucidated. This employs a voltage follower cell called Flipped Voltage Follower (FVF) [20] based current mirror and current comparator configurations in ADC design, thereby improving its performance in terms of supply voltage requirement, power dissipation reduction and faster conversion rate.

2. FVF [20]

FVF is essentially a source follower circuit wherein shunt feedback and current biasing have been employed, as depicted in the basic PMOS FVF cell of Fig. 1. This simple circuit works independently of the supply voltage [21].

As shown in the Fig. 1, there are two pMOS transistors MF1 and MF2 with shunt feedback. Owing to this shunt feedback, transistor MF2 remains ON, irrespective of the power supply is given to the circuit. When an input current is applied with all transistors biased in the saturation region, then shunt feedback provided by transistor M2 causes the impedance at the input node to be very low and, so the amount of current flowing into this node does not modify the value of the voltage developed at this node. Thus, the input node is capable of sourcing large current variations at the input and the FVF then translates them into compressed voltage variations at output node.

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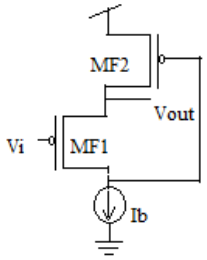


Fig. 1 Basic FVF (PMOS) cell

Thus, the input node is capable of sourcing large current variations at the input and the FVF then translates them into compressed voltage variations at output node. Feedback in the FVF allows low impedance at the output node given by-

$$r_o = \frac{1}{g_{m1} g_{m2} r_{o1}} \quad (1)$$

where gm1 and gm2 are the transconductances of transistors MF1 and MF2 respectively and ro1 is the output resistance of transistor MF1 [20]. This low output impedance is conducive for sourcing a large amount of current.

The FVF can also be configured as a current sensor cell, as depicted in Fig. 2. The shunt feedback provided by MC2 makes the impedance at the input node very low and its value is given by [20].

$$r_x = \frac{1}{g_{mc1} g_{mc2} r_{o1}} \quad (2)$$

Therefore, the voltage at node ‘X’ remains almost unchanged by the amount of current flowing into this node. This node is capable of sourcing large current variations at the

input which are translated into corresponding voltage variations at output node 'Y' by the means of FVF. This voltage can then be used to mirror the input current via transistor Mcout. This establishes the basis of current mirroring concept using FVF.

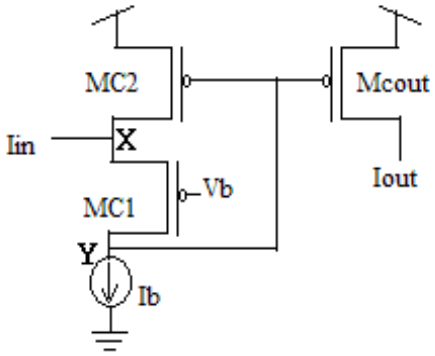


Fig. 2 FVF current sensor cell (PMOS Type)

The output and the input currents can be estimated from the dc response of this current sensor cell [20] and are found to be related as

$$I_{out} = I_{in} + I_b \qquad (3)$$

The current Ib, (bias current) can be easily removed from the output node using current mirroring techniques as described in [20]. In the following section the concept of current sensing FVF cell is used in implementing current-mode ADC.

3. Proposed Current-Mode ADC Structure-Design and Operation

A generic n-bit current-mode flash ADC consists of 2n–1 comparators with each comparator comparing the input to a progressively increasing reference current level such that each successive level is 1 LSB higher than the previous one. The 2n–1 comparator outputs form a thermometer code which is then processed by an encoder to generate an n-bit binary output [23].

Specifically, in a 2-bit current-mode flash ADC, as implemented in this paper, the analog input current range is divided into 2*2-1 = 3 set values which are designated as reference currents. These reference currents serve as one of the fixed inputs to the current comparators used in the design. There upon, the input current is applied to the ADC input. This input is compared to the different reference currents in their respective current comparators. Based on the result of the comparison, an output code, called thermometer code (as discussed above) is generated. This code is then fed to a suitably sized encoder (3X2 for a 2-bit ADC) to obtain the final digital output. Fig. 3 shows the basic scheme of the proposed 2 bit current-mode flash ADC, which has four main units: FVF based input stage and current comparators, a reference current generating structure, and an encoder. The working of these stages is discussed in the following sections.

3.1 FVF based input stage

The function of the input stage is to provide 2n-1 identical copies of the input current, where n is the number of binary outputs which for a 2-bit ADC is equal to 2. Thus, the input stage in this implementation produces (2*2-1=3) identical copies of input current. This is achieved by using a current sensor followed by a current replicating structure. In our proposed circuit, the input current Iin is being sensed using FVF current sensing feature as discussed in reference to Fig. 2 in the section 2. The current Iin is then replicated through transistors M3, M4 and M5 [24].

3.2 Reference Current generating structure

The Reference Current generating structure provides progressively increasing reference currents for comparison purpose. The reference current values are computed as follows:

For an input current ranging from Imin to Imax, the step size is calculated as

$$Step = \frac{I_{max} - I_{min}}{2^n - 1} \qquad (4)$$

The reference currents are calculated as

$$I_{refn} = Step.i \qquad (5)$$

where i= 1, 2,…….2n-1. Thus, for a 2-bit ADC, the three values of reference current (2n-1 = 3) required would be:

$$I_{ref1} = Step$$
$$I_{ref2} = Step.2 \quad (6)$$
$$I_{ref3} = Step.3$$

The reference current generating structure of Fig. 3 consists of transistors M6-M10, wherein M6 and M7 set up a DC reference current that is reproduced in M8–M10 to establish the desired reference current Irefi by suitably increasing aspect ratios of M8–M10. This is done by keeping the channel length same for all these transistors while increasing the widths of transistors by a factor of Δ, i.e. width of transistors M8-M10 are W, W•Δ and W•2Δ.

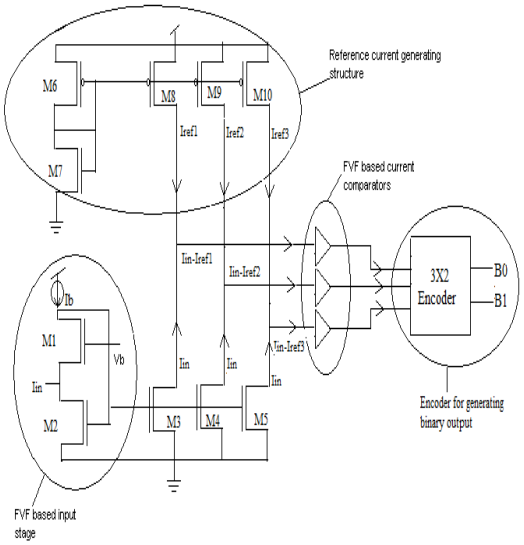


Fig. 3 Basic scheme of proposed 2 bit current-mode flash ADC

3.3 *FVF based current comparator*

The schema uses an FVF based current comparator proposed by the authors, illustrated in Fig. 4. The operation of this FVF based current comparator is explained in this section. The input to the current comparator is the difference between the input current I_{in} and the reference current I_{refi} i.e. I_{in}-Irefi = I_d, say, obtained from the input current mirror and reference current generating structure.

The comparator employs an FVF based source follower (MF1-MF2) as the input stage, followed by a CMOS inverter (MF3-MF4) so as to attain sufficient gain that can amplify small voltage variation occurring at the input stage. The source follower offers low input resistance which is given by

$$r_{in} = \frac{1}{g_{mF1} g_{mF2} r_{o1}} \quad (7)$$

The current applied to the input node of the current comparator is translated into corresponding voltage variations at the node 'Z'. These small voltage variations at 'Z' are amplified using a positive voltage feedback from the CMOS inverter. Further, a chain of two CMOS inverters (MF5-MF6 and MF7-MF8) is added to obtain full rail-to-rail swing. Based on the value of I_d, the circuit operation can be divided in 2 modes. In first mode, when I_d is positive, the output of the FVF source follower stage is high. The CMOS inverters chain amplifies this output to obtain a rail-to-rail swing, hence generating the overall output of the current comparator a high. In the second mode, when I_d is negative, the output of the FVF source follower stage is low and the overall output of the current comparator from the CMOS inverter chain, with rail-to-rail swing, is a low.

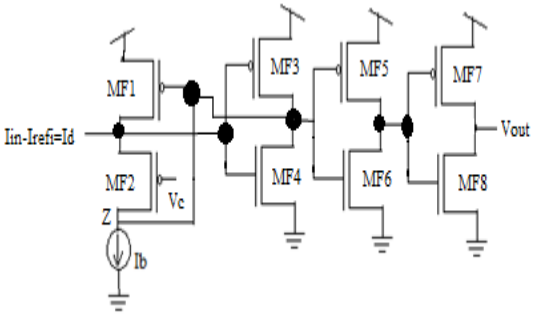


Fig. 4 FVF based Current Comparator

4. ENCODER

The outputs of the current comparators are fed into an encoder that generates binary output corresponding to applied analog input. For 2-bit binary output, a 3X2 CMOS Transmission gate based encoder, illustrated

in Fig. 5, is used. Table 1 shows the truth table for the same.

Table 1. Truth Table for 3X2 encoder

Comparator Outputs			Encoder Outputs	
C1	C2	C3	B1	B0
0	0	1	0	1
0	1	1	1	0
1	1	1	1	1

The expression for B1 and B0 as obtained from the truth table of Table 1 are-

$$B1 = C2 \text{ AND } C3 \quad (8)$$

$$B0 = C3 \text{ AND } (C1 \text{ XNOR } C2) \quad (9)$$

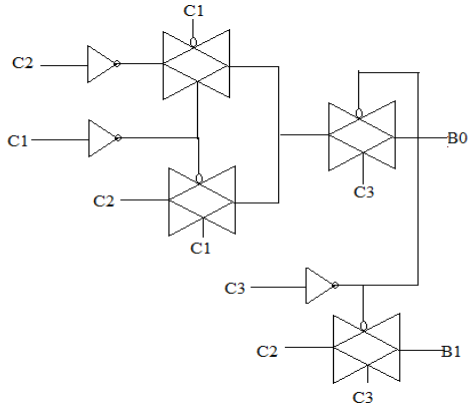
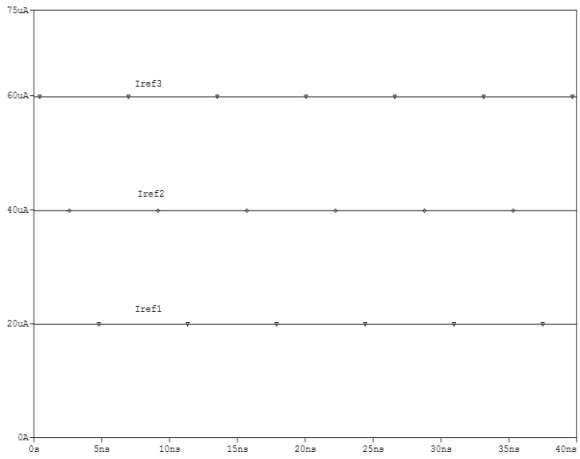


Fig. 5 3X2 CMOS transmission gate based encoder.

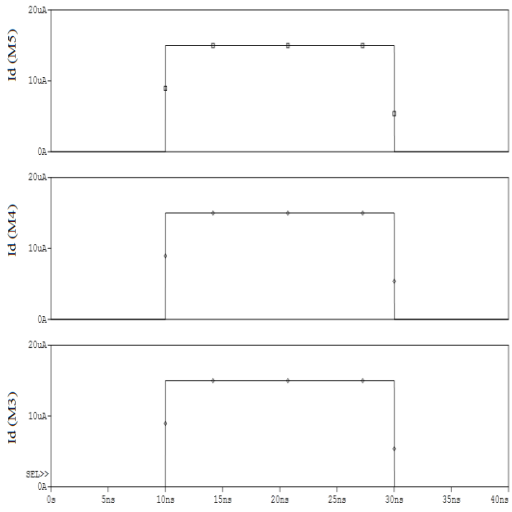
5. SIMULATION RESULTS

To examine the concepts described above, the circuit shown in Fig. 3 was simulated using a 0.18 µm TSMC CMOS technology parameters and power supply of 1.8 V. The functionality of FVF based input stage and current comparators, a reference current generating structure, and an encoder is verified first and then overall operation of the. ADC was tested for an input current range of 0-60µA. The aspect ratios have been fixed in accordance with Table 2, to obtain I_{in}-I_{ref1}= 5 µA, I_{in}-I_{ref2}= 25 µA and I_{in}-I_{ref3}= 45 µA. The delay observed in the generation of I_{in}-I_{refi} from the input stage and reference current generating stage is observed as 1.5ns.

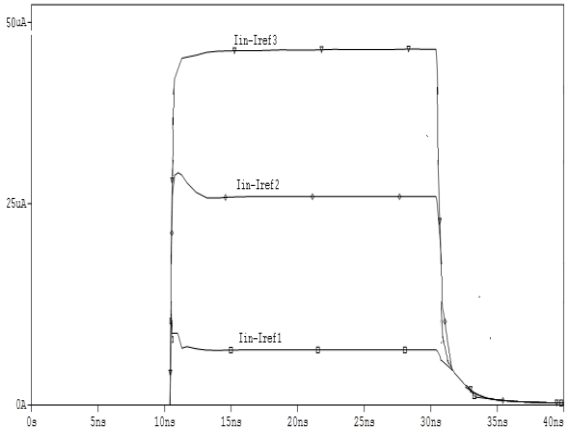
The outputs of each stage have been illustrated in the Fig. 6, 7 and 8 below. Fig. 6(a) demonstrates the generation of I_{refi} from the reference generating stage. It can be seen from the Fig. 6 (a) that this stage produces three progressively increasing reference current values of 25 µA, 35 µA and 45 µA respectively. Simultaneously, three identical input current values are obtained from the FVF based input stage, as depicted in Fig. 6(b). For our implementation, we have varied the input current I_{in} over the range of 0 to 60 µA. Further, the I_{in}-I_{refi} from the input stage and reference current generating stage has been depicted in Fig. 6(c). Further, the FVF based current comparator structure was simulated for an exemplary input current difference value of 15µA, for a supply voltage of 1.8V. Fig. 7 depicts the input waveform and the output response of the FVF based current comparator. The propagation delay offered by the current comparator when operating as a stand-alone circuit is observed to be 3.5 ns and the power dissipation is of the order of 25 µW.



(a)



(b)



(c)

Fig. 6 a) Output of Reference generating stage b) Output of FVF based input stage c) I_{in}-I_{refi} generation from input stage and reference current generating stage

Table 2 Aspect Ratios of transistors

Transistor	Width (µm)	Length (µm)
M1	5.4	.27
M2	5.4	.27
M3	2.7	.27
M4	2.7	.27
M5	2.7	.27
M6	2.7	.27
M7	.27	.73
M8	1.5	.27
M9	3	.27
M10	6	.27

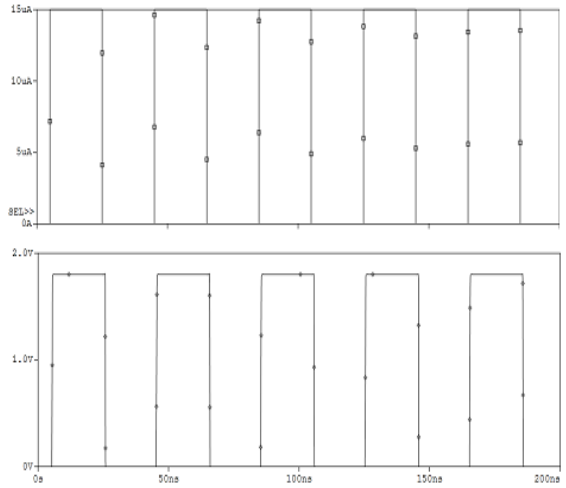


Fig. 7 Input (I_{in}-I_{refi}) to the FVF based current comparator and the corresponding output response.

Fig. 8 shows the outputs of all the four stages corresponding to 2-bit ADC outputs i.e. B0 and B1 when a slowly increasing input current from 0-60µA was applied. It is seen that for this input current, the corresponding digital outputs obtained are in accordance with the Table 1. The circuit has a conversion time of 12ns for 2-bit conversion.

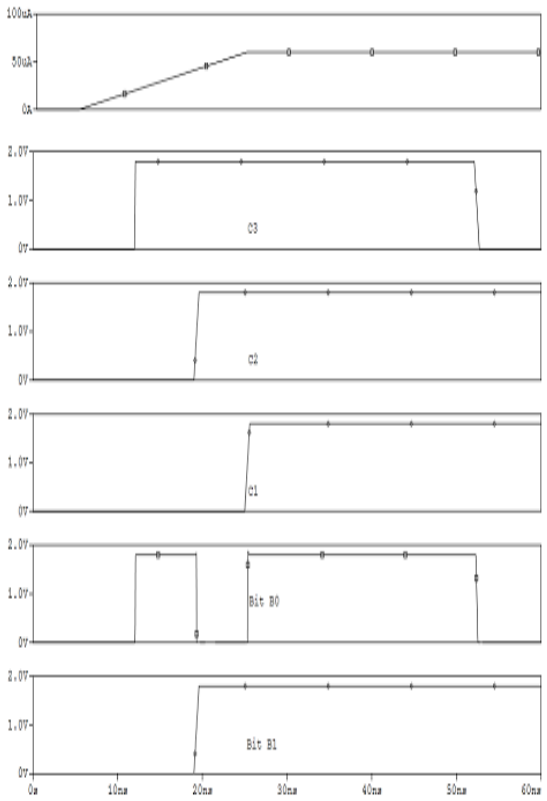


Fig. 8 2-bit ADC output for 0-60µA input current

Fig. 9 shows the plot of the specifications of the 2-bit ADC implemented. The specifications are summarized in Table 3.

Table 3. 2-bit ADC specifications

Parameter	**Value**
Offset	6 µA
INL	0.75LSB
DNL	0.6LSB

Further, Fig. 10 shows the current difference (I_{in}-I_{refi}) versus propagation delay plot for complete 2-bit ADC conversion. Assuming the propagation delay of input stage and the encoder constant, it is observed that for larger current difference input, the propagation delay is smaller due to faster switching of current comparator at higher currents.

6. CONCLUSION

A 2-bit Flipped Voltage Follower based Current-mode ADC using current instead of voltage to represent the signal is designed and implemented using PSPICE in 0.18µm CMOS technology. The ADC is expandable up to n-bits. The circuit has a conversion time of 12ns for complete 2-bit conversion. However, as the number of bits desired increases, the conversion time also increases. The currents are susceptible to process technology and temperature variations. This may adversely affect the current matching in current mirrors. So, the final output may become function of temperature. Nevertheless, the simulation results demonstrate the feasibility of the proposed design by exhibiting satisfactory response and quick conversion time.

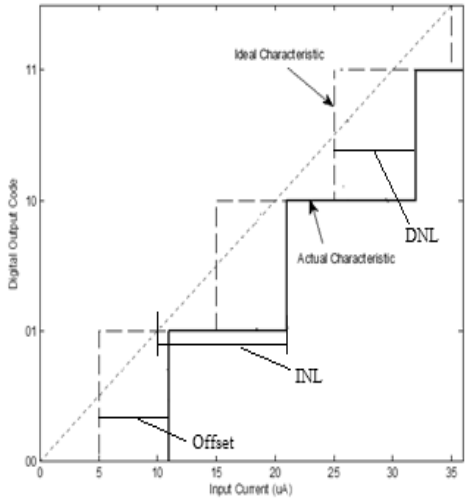


Fig. 9 Specifications of the 2-bit ADC

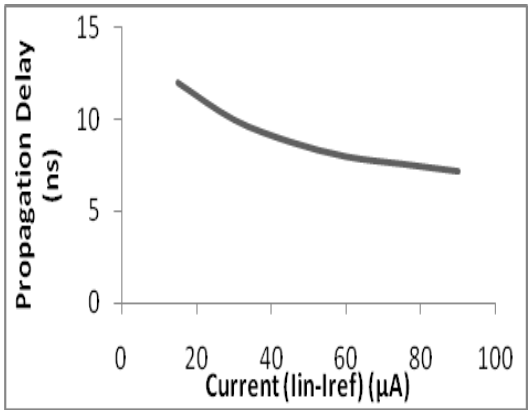


Fig. 10 Input current difference versus propagation delay plot for 2-bit ADC conversion

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