Comparitive Analysis and Optimization of Current Mirror-An Overview

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Abstract:

This paper presents the comparison and optimization of different types of current mirrors using CMOS and Bi-CMOS technology with requirements to operate with lower voltage and currents in the range of microamperes to Pico amperes. An overview of traditional current mirror configurations is presented and a highly accurate, wide swing Bi-CMOS and CMOS cascode current mirror is proposed. Details of the proposed configuration are provided and the improvements that will be achieved through Bi-CMOS technology are indicated. Also included are the future plans to continue evaluating and refining the proposed structure.

Keywords: Current mirror, CMOS, Bi-CMOS low power design

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1. Introduction

The rising production of portable electronics has increased the need for low power, low voltage devices. One possible approach to achieve this goal is by designing power efficient, low voltage base components and building blocks.

Current mirror is a very useful building block in analog integrated circuit design. It is widely used in the biasing circuits and constant current generation circuits. In many analog circuit applications, the performance of the current mirror focuses on the high accuracy, high output impedance, wide output voltage range, wide current mirroring range, and fast current switching time. Many fundamental current mirror configurations have been developed in bipolar, MOS, and Bi-CMOS technologies. In this paper we describe the work in progress to develop a Bi-CMOS CM configuration. Bi-CMOS has high output impedance by using npn-NMOS cascode. Compared to other topologies, this circuit topology offers several advantages. These advantages include ease of design, close to ideal mirroring, insensitivity to the power supply variations of the mirrored currents, and good operational insensitivity to process parameter variations, thereby requiring no trimming or self-calibration.

This paper has been organized as follows. In the section 2, traditional CM configurations in MOS technologies are reviewed. Section 3 presents a discussion of salient Bi-CMOS implementations. Next, a discussion of the proposed Bi-CMOS and CMOS current mirror is presented.

1.1 The Traditional Current Mirror

The basic idea underlying a Current Mirror (CM) is the assumption that one precisely defined current source is available and other current sources copy their current from this precise current source.In other words CM uses the principle that if the gate source potential of two identical MOS transistors is equal, then the channel current should also be equal.

For instance, we know that $I_d = f(V_{GS})$, so $V_{GS} = f^{1}(I_d)$. Now if a transistor is biased at I_{ref} then $V_{GS1}=f^{1}(I_{ref})$ and $Io=f(V_{GS2})$ because $V_{GS1}=V_{GS2}$ $I_o=f\{f^{1}(I_{ref})\}$, So $I_o=I_{ref}$

In others words if two identical MOS devices that have equal gate source voltage are operated in saturation then they carry equal current.

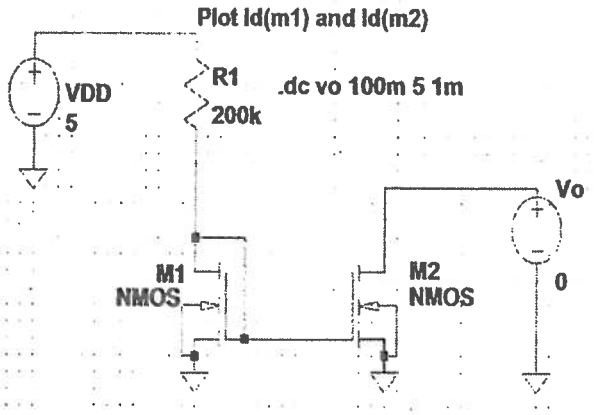

Figure 1: Basic current mirror

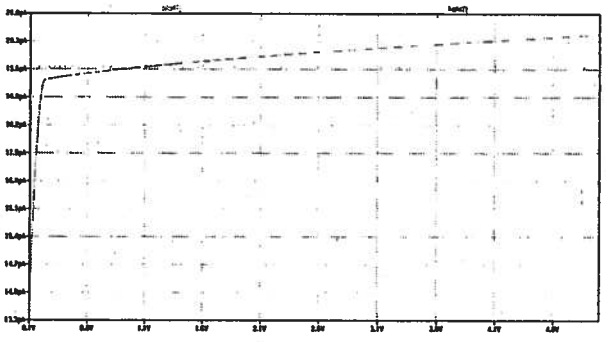

Figure 2: Basic CM output current

1.2 The Bi-CMOS Current Mirror

With the increasing acceptance of BiCMOS technology, several approaches have been reported to overcome the deficiencies identified in traditional approaches.

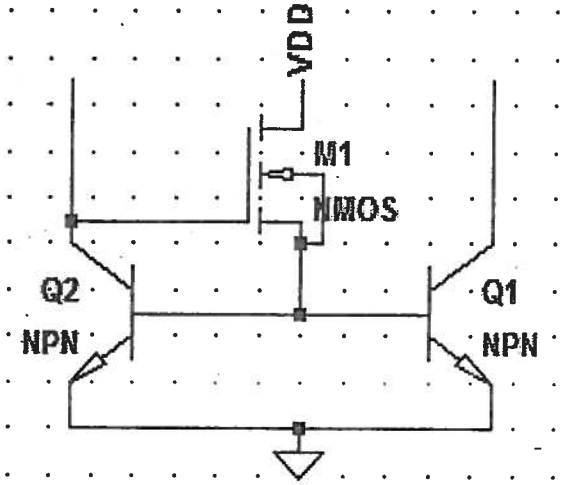

Figure 3: Sasaki's current mirror

A low power BiCMOS current mirror configuration was proposed by Sasaki et al is shown in Figure 3.

The second configuration is based on the MOS Wilson current mirror. It replaces the top MOS transistor with a bipolar (Q1), as shown in Figure 4.

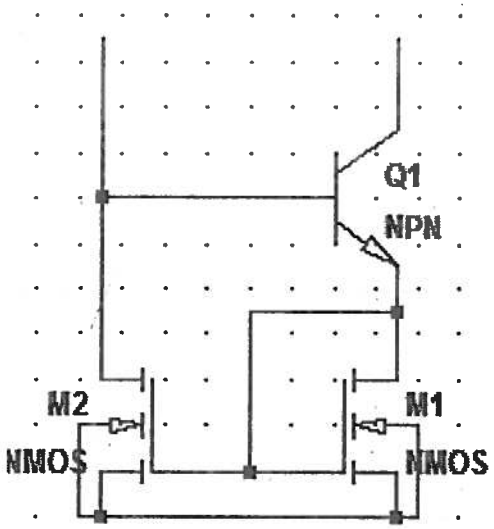

Figure 4: BiCMOS Wilson Current

The configuration will need low input voltage because the base-emitter junction voltage of a bipolar transistor is smaller than the gate source junction voltage for a MOS. Thus this design is also expected to achieve stability at low supply voltages and small currents requirements.

2 The Proposed Bi-CMOS CM

Fig. 5 shows the proposed BiCMOS cascade current mirrors. The current mirror in Fig. 5 is the BiCMOS cascade current mirror with a collector voltage matching circuit.

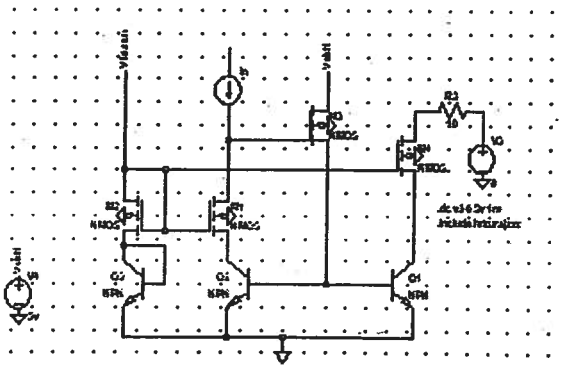

Figure 5: Proposed Bi-CMOS current mirror with collector voltage matching circuit

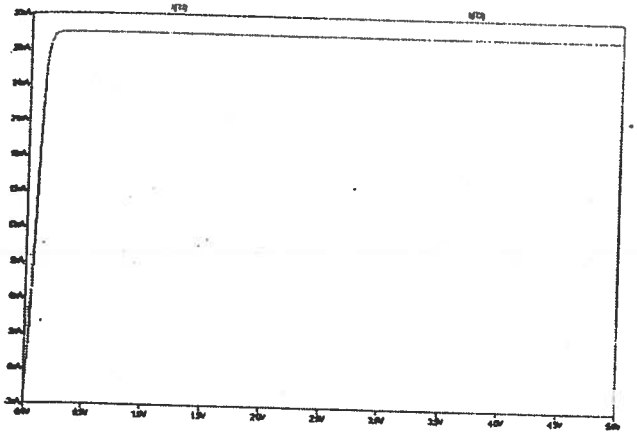

Figure 6: Proposed Bi-CMOS CM output current

The BiCMOS-CM is based on the BJT current mirror with an NMOS transistor in Fig. 5 to compensate the base current error. The base-current compensated BJT current mirror has low minimum output voltage (V) and fast current settling time. To overcome the disadvantage of the base-current compensated BJT current mirror, the npn-NMOS cascade structure is used in the current output. The npn-NMOS cascade structure is chosen instead of the npn-npn cascade structure. The output impedance of the npn-NMOS cascade is smaller than that of the npn-npn cascade structure. However, in npn-npn cascade structure, the second npn transistor needs the second base current and it causes the current mirroring error. In the Bi-CMOS CM, three currents flow, which are I_{IN}, $I_{OUT}=M\times I_{IN}$, $I_{BIAS}=1/K\times I_{IN}$. The transistor size ratio in the three current paths of I_{IN}, I_{OUT}, and I_{BIAS} is 1:M:1/K. The gate-source voltages of M1, M2, and M3 are the same, because the transistor size ratio and the current ratio in three transistors are the same. Also, the collector emitter voltages of Q1, Q2, and Q3 are the same due to the same transistor size ratio and the current ratio. Therefore, the base, collector, and emitter voltages of Q1 and Q2 are perfectly matched. The Bi-CMOS CM mirrors the input current exactly.

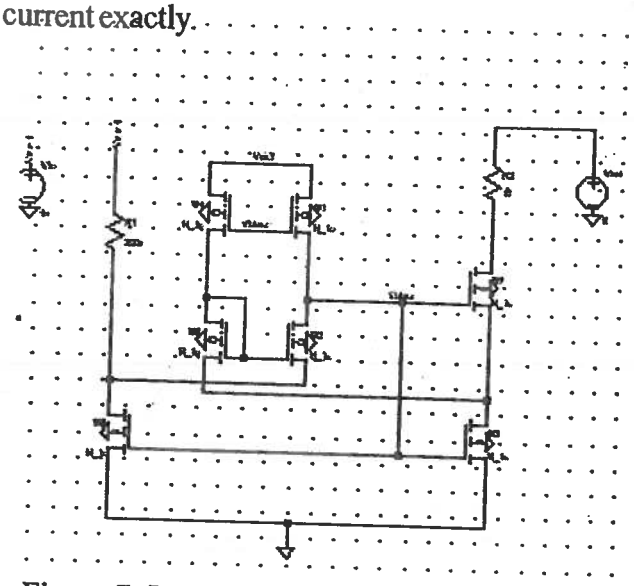

Figure 7: Proposed CMOS current mirror

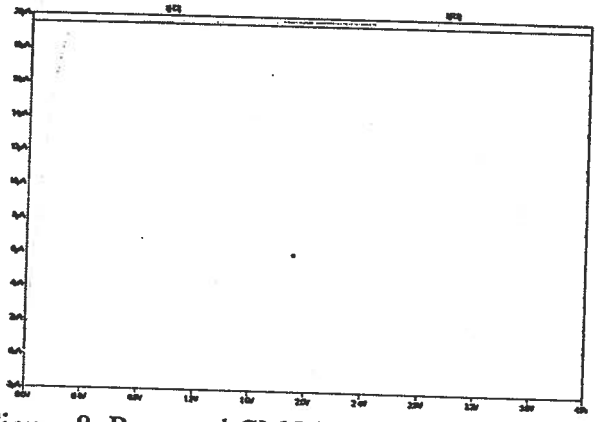

Figure 8: Proposed CMOS CM output current

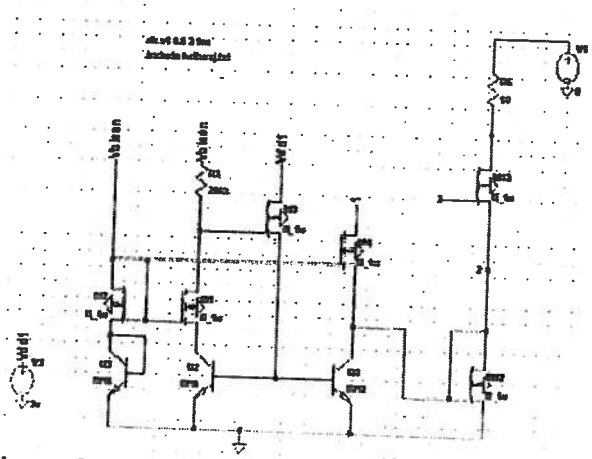

Figure 9: Proposed Bi-CMOS CM with AND GATE configuration

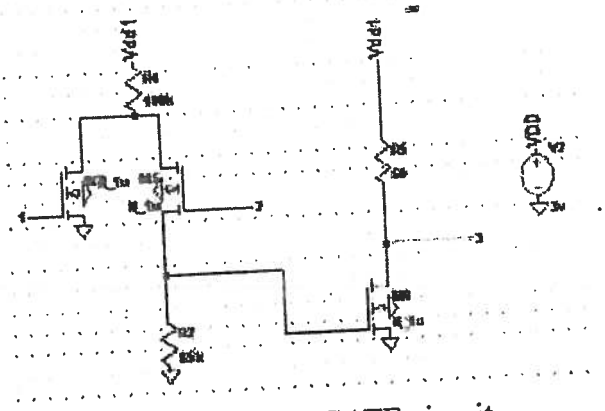

Figure 10: AND GATE circuit

2.1 Simulation Results

The proposed circuits (Figs. 5, 7 and 9) were simulated for 1 μm technology with level 4 parameters. For Fig. 6, I_{bias} are assumed to be 27.628nA and for Fig. 7 I_{bias} are assumed to be 19.48uA. Selection criterion for I_{bias} is to ensure lower V_{in} and I_{offset}. All the circuit operations were simulated for the supply voltage ±3.0 V. The small signal output impedance, which is a function of I_{out} is around 7.39G for Bi-CMOS CM and 117.55M for CMOS CM The bi-CMOS structure consumes 2.977nW power and CMOS consumes 78.15uW. The *V*in versus *I*in characteristics is shown in Fig. 6 and 8.

3. Conclusion

A highly accurate wide swing Bi-CMOS and CMOS cascode current mirror is proposed and implemented. The proposed Bi-CMOS CM uses the base-current compensated BJT current mirror. Also, the npn-NMOS cascode is used to increase the output impedance and to reduce the minimum output voltage. The NMOS transistor controls the collector voltage of the npn current mirror device for the accurate current mirroring with the collector voltage matching circuit and the collector voltage control circuit in the Bi-CMOS CM. The proposed current mirrors achieve the highly constant current for wide output voltage range. It is expected that the proposed current mirrors can be applied to not only to low voltage but also high voltage circuit applications. They can be useful for display driver circuits such as LED driver circuits with fast current switching for with wide output voltage range.

The ever-rising proliferation of portable electronics has increased the need for low power, low voltage devices. One possible approach to achieve this goal is by designing power efficient, low voltage base components and building blocks. This would enable to achieve both higher integration levels in VLSI technology and more power-efficient systems. Current mirrors are one of the building blocks more widely used in many applications. However, they usually require either a relatively high voltage or input current to operate properly. Thus, new current mirrors that consume less power will serve well the increasing need for low power consuming building blocks.

4. Future Work

This research is still in progress. Currently, the models of the transistors to be used to simulate the current mirrors are under development. In the next stages of this work, the proposed current mirror will be simulated for establishing its sensitivity, voltage and current requirements, temperature dependence, dependence on the transistor beta and Early Effect and other measures that would allow comparing its performance with other established configurations. The circuit can be used as a building block in low voltage mixed-signal VLSI systems.

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