PERFORMANCE EVALUATION OF HYBRID FPGA ARCHITECTURE FOR RECONFIGURABLE COMPUTING SYSTEM

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ABSTRACT

High Performance Computing (HPC) applications demand high performance from reconfigurable computing systems (RCS). Reconfigurable architectures can adapt to the behaviour of the hardware resources meant for a specific application. Computing using reconfigurable architectures provides a method to utilize the available logic resources on the chip for various computations. The basic ability of reconfigurable computing is to perform computations in hardware to increase performance, while still retaining the flexibility of the application software. The purpose of this paper is to evaluate the performance of reconfigurable computing system using Hybrid architecture involving two main types of programmable logic devices, field-programmable gate arrays (FPGA) based on LUTs technology and complex programmable logic device (CPLD) based on PLAs technology. They are both widely used. Each technology has strength in the particular areas of reconfigurable system design. We identified these architectures as Hybrid Reconfigurable Computing Architectures (HRCA). The basis of the HRCA is that some parts of digital circuits are well-suited for execution with LUTs, but other parts the PLAs structures are more useful. For several classes of high performance applications, the new architecture HRCA offers significant savings in total logic area in comparison with an architecture containing only LUTs. It also offers some improvements in speed performance. The main focus of this paper is on summarizing the methodologies required to understand the prospective of hybrid architecture with respect to conventional architecture for reconfigurable computing in the term of models, size and power.

Key word: *Reconfigurable computing, FPGA, CPLD, hybrid architecture.*

1. INTRODUCTION

Research in the field of reconfigurable computing is increasing speedily in the area of computing science and electronic engineering. Basically, there are two main principles in conventional computing for the execution of high performance applications. The first is Application Specific Integrated Circuit (ASIC) which is designed for a specific application with fixed functionality, and is therefore it is very fast and efficient. Microprocessors are a far more flexible solution. Processors execute a set of instructions to perform a computation. By changing the software instructions, the functionality of the system is altered without changing the hardware. As we know that the microprocessors are the heart of most high performance computing architecture or platform. They provide a flexible computing platform and are able to execute a large category of applications. Unfortunately, this flexibility decreases the performance of application. ASICs give an alternate solution which solves the performance issues of general purpose microprocessors. Hence, every ASIC has fixed functionality with greater performance over controlled set of applications. The second is reconfigurable computing which fills the gap between hardware and software. Reconfigurable computing utilizes hardware resources that can be tailored at run-time to give greater flexibility without compromising on performance. Reconfigurable computing devices agree to assemble both requirements i.e. flexibility and performance. Reconfigurable systems have evolved from Field Programmable Gate Arrays (FPGAs).

Presently there are a large class of FPGAs developed by different vendors namely Xilinx and Altera. Different types of computing systems have been constructed by integrating FPGAs with dedicated memory, general purpose microprocessor

or an ASIC like as Digital Signal Processor (DSP) on a given platform. The entire components are communicated through communication buses. But for high performance application, we need to improve the communication and memory access for configuration and data. Future reconfigurable systems are integrating reconfigurable logic onto the same chip as microprocessor. This architecture can be known as hybrid reconfigurable computing architecture (HRCA). In this architecture it can distribute the computations between different components(LUT/PLAs) of the system to improve the overall computing performance and logic concentration.

2. RELATED RESEARCH WORK

Field Programmable Devices (FPDs) face many challenges from lower speed-performance and less logic capacity in comparison to custom manufactured technologies, such as mask-programmed gate arrays. However, a lot of research has been devoted to improving FPD architecture. New architecture continues to emerge as main research in industry and academia with advanced total logic capacity and better speed-performance. A highlight of some recent research efforts on FPGA logic blocks is presented here.

Logic synthesis targeting FPGAs has been researched extensively and numerous technology mapping approaches for LUT based FPGAs have been developed. These approaches have two main objectives, area and delay minimization [5].

In many reconfigurable embedded systems size, power and cost optimizations are the central goals. In those systems the growing need of more computation power that contradicts with size, power and cost optimization puts a lot of pressure on researchers who must discover a good balance of all contradicting goals. In the July 2005 edition of the Altera Stratix Device Handbook[6], Stratix is an SRAM-based island-style FPGA containing many mixed computational elements. The main element is the logic array block (LAB), which contains 10 logic elements (LEs). The general architecture of the LE is much related to the structure that we use to develop an HRCA, i.e. single 4-LUT function generator and a programmable register. The FPGA research done by J.Rose, focused on logic-block density. Assuming a LUT-based architecture, authors change the number of inputs to a LUT to measure the effects on implementation of a benchmark circuit set. Their conclusion is that LUTs with 4 or 5 inputs yield the best results in terms of chip area. We try to apply this result by using 4-LUTs, which are also found in commercial FPGAs such as the Altera Flex 10K, and the Xilinx Virtex. [7]. Multicontext programming bits, a scheme that promises some savings in area efficiency and reconfiguration time for FPGAs was proposed by E. Tau et al. in their research [8]. In the research of Altera industry, they have recently introduced the new series of field programmable devices (FPDs) known as APEX (Advanced Programmable Embedded Matrix). Their main characteristic is the combination of LUTs and PLA like blocks on the same chip. APEX architecture contains embedded system blocks that can be configured to support pterms, memory blocks and content addressable memory cells (CAMs).The first APEX devices will offer 500,000 gates, but in future they plan to include some more devices up to 2 million programmable gates [9]. In the study of J. He and J. Rose, called Heterogeneous FPGAs, they investigated FPGA architectures with logic blocks of two different sizes to see the effects on area efficiency of LUT-based FPGAs on the same chip. In the result they provide a saving of 15% in chip area by mixture of LUTs [12]. Most of the research focused on FPGA based FPDs rather than CPLD based FPDs. The published work in the area of CPLDs research is still small. Though, in the study of J. L. Kouloheris and A. El Gamal, they investigated and built FPDs using PLA based logic blocks. According to authors, an FPD based PLAs with 10 inputs, 12 Pterms, and 3 outputs achieves about the same level of logic density as FPGAs based on 4-LUTs, but this unchanging share decreases the flexibility of FPGA. We are not aware of any industrial product that is based on such FPDs based PLAs. [13]. S. Wilton et. al. explain the memory modules with variable aspect-ratio that could be incorporated as separate blocks in an FPGA. This design is not orthogonal to the Hybrid FPGA, and so memory blocks could also be included in our

architecture for delay minimization [14].

In the Altera data sheet, implementations of partial logic circuits with PLAs are also founded in commercial FPGAs. An Embedded System Block (ESB) of Altera APEX20K can be configured as a PLA with 32 inputs, 32 product terms(pterms) and 16 outputs [10]. In the same way, in every Xilinx Virtex II slice has a devoted OR gate named ORCY, with which a Configurable Logic Block (CLB) can implement 2 product terms with 16 inputs [11]. These architectures are beneficial to the logic density of FPGA. However, they are not optimized specifically for implementing PLA. Microelectronics Center of North Carolina (MCNC) benchmark suite is used as logic synthesis and optimization benchmark. The benchmark suite has standardized libraries with representative circuit designs ranging from simple circuits to advanced circuits. MCNC benchmarks are very popular in academic research. The FPGA researcher relies a lot on benchmarks to evaluate performance of their hardware and software solutions. Hence standard and fair benchmarking practices are essential to calculate FPGA architecture, design configuration, verification and validation of FPGA device and to verify their potential to support target applications. In this paper we try to use some MCNC bench mark to evaluate the architectural performance of HRCA.

3. RECONFIGURABLE COMPUTING

Reconfigurable computing is a relatively new field of research and development, the first research beginning in the late 1980's. It is an effort to overpass the traditional gap between hardware and software within the computing field. Reconfigurable Computing is emerging as an important replacement for computing algorithms evolved from FPGA. The key feature of this is that it incorporates the performance of ASIC and flexibility of GP (General-Purpose) processors. These devices are composed of logic device FPGA (Field-Programmable Gate Array), which help in determining functionality of the system from programmable configuration bits. Modern high-end FPGAs can have tens of millions of configuration points. FPGA consists of matrix of logic blocks and interconnection network between the logic block. The functionality of logic blocks and its interconnection can be customized by downloading bits of reconfiguration data on the given hardware[3][4]. In FPGA, the resources needed for the computation of an application will be built as components to be downloaded to the device at run-time. The generation of such components is called logic synthesis. Reconfigurable devices are usually used in three different ways:

• **Rapid prototyping**: The reconfigurable device is used as an emulator for another digital device, generally an ASIC.

• **Non- regularly reconfigurable systems**: The reconfigurable device is integrated in a running system where it is used as an application-specific processor. These systems are usually individual systems.

• **Regularly reconfigurable systems**: This third category comprises of systems which are frequently reconfigured. These systems are usually coupled with a host processor which is used to reconfigure the device and control the complete system

Depending on the time at which the configuration sequences are defined, the computation and configuration flow of data on reconfigurable devices can be classified into two categories:

• **Compile-time reconfiguration**: In this case the computation and configuration sequences as well as the data exchange are defined at compile time and never change during a computation.

• **Run-time reconfiguration:** The computation and configuration sequences are not known at compile time. Request to implement a given task is known at run-time and should be handled dynamically.

4. ARCHITECTURE OF CPLD/FPGAS

The two main types of programmable devices, field programmable gate arrays (FPGA) and complex

programmable logic devices (CPLD), are both extensively used. Each device contributes particular strength in the development of reconfigurable system. FPGAs programmed with static RAM technology are usually based on lookup tables. A look up table (LUT) is a group of memory cells, which contain all possible results of a given function for a given set of input values. An n-input LUT can be used to implement up to different functions, each of which can take 2^n possible values[3].

In FPGA, a LUT physically consists of a set of SRAM cells to store the value and decoder that is used to access the correct SRAM location to retrieve the result of functions Figure 1 (b). Their main strengths are very high logic capacity in the range of hundreds of thousands of equivalent logic gates and good speed performance up to 20-50 MHz system clock rates. SRAM based LUT is used in the most commercial FPGA as function generator[2][18].

(2) On the other hand, CPLDs consist of a set of macro cells, input/output blocks and an interconnection network. A macro cell typically contains several PLAs and flip flops. Programmable logic arrays (PLA) consist of a plane of AND-gates connected to a plane of OR-gates and both the planes can be programmed by the user Figure 1 (a).

Their characteristics include medium capacity in the

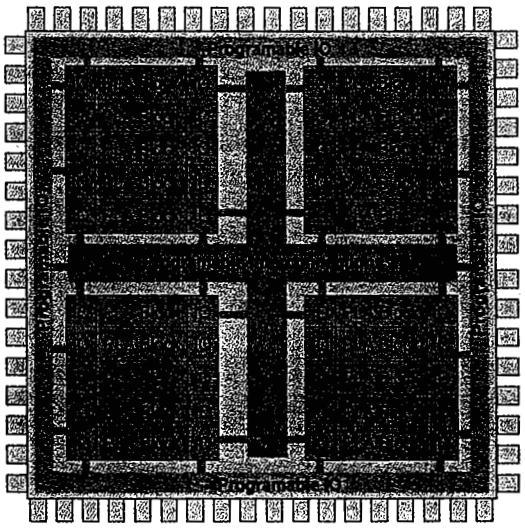

Figure 1 (a): CPLD Device

range of a few thousand gates, and ultrahigh speed performance, sometimes in excess of a 140-180 MHz system clock rate[16].

HRCA merge the two common technologies

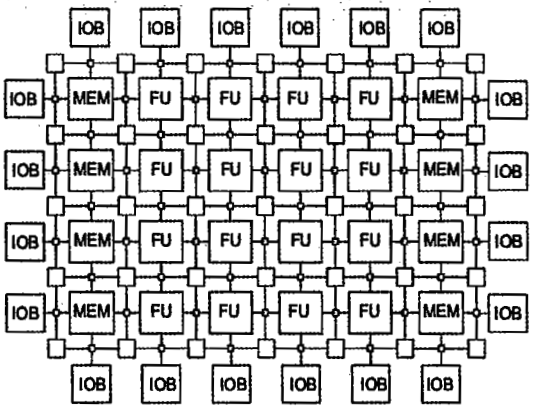

Figure 1 (b): FPGA Device

used in programmable logic devices: lookup table (LUT) based FPGA and PLA – like logic cell based CPLD. The most important initiative is to find out what functions are suitable to be implemented on which logic resources. Logic resources include LUTs as well as product term (pterm) like PLA logic cells. In this paper we analyse the performance of HRCA in comparison with an architecture containing only LUTs. It indicates that the new architecture offers significant savings in total chip area. Also, the HRCA can reduce the depth of circuits implemented in the FPGA, which may provide improvements in data communication speed and performance.

5. HYBRID ARCHITECTURE

Reconfigurable computing systems regularly show remarkable performance and strength in terms of

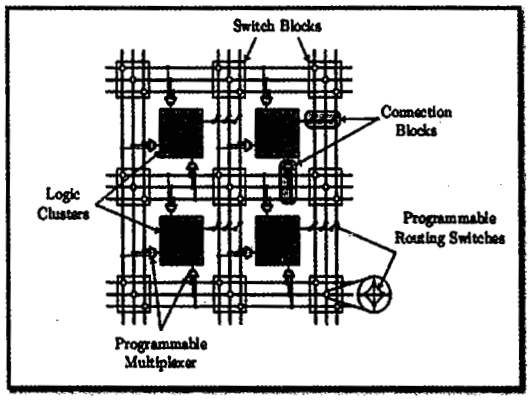

Figure2: Structure of Switch and Connection Block

high speed, reduced energy and power consumption.

The advances in high-performance

computing and reconfigurable computing based on field programmable gate arrays (FPGAs), form the basis for a new paradigm called reconfigurable supercomputing. This can be achieved through hybrid of LUTs and PLAs of programmable logic devices.

FPGA programmed with SRAM technology are usually based on Look-Up Tables (LUTs). For implementing random logic circuits in LUT based FPGA, the cost of LUTs increases exponentially according to the inputs of circuits. So LUT is suitable for **low fan-in logic circuits**. CPLDs are based on Programmable Logic Arrays (PLAs). A PLA usually has tens of inputs and is appropriate for **high fan-in logic circuits**. CPLDs are typically faster and have more predictable timing than FPGAs because FPGAs are generally more dense and contain more flip flops and registers than CPLDs[1][15].

As in most of the applications, due to fine granularity of FPGA most of the connections in Connection Blocks (CB) are never used and many Logic Blocks (LB) are used. So a large percentage of chip area is wasted. To rectify the above drawbacks, it has been tried to develop a new structure of connection Blocks (CB) which will facilitate to work in LUTs mode or PLAs mode for algorithm computation depending upon circuit fan-in (Figure 2.)

Hybrid Reconfigurable architecture additionally contains multiple level configurability and can accomplish the reduction of compilation and synthesis to a single step. It can be reconfigured at multiple levels of abstraction at which computations are implemented, i.e. the computational hierarchy.

6. FACTORS FOR PERFORMANCE ANALYZING HYBRID ARCHITECTURES.

Hybrid architecture is based on the mixture of two existing configuration technologies: Field Programmable Gate Arrays (FPGAs) based on Look Up Tables (LUTs), and Complex Programmable Logic Devices based on PALs/PLAs. As we know PLAs are suitable for the operation of large fan-in logic circuits, while LUTs are used to execute low fan-in logic circuits. In the traditional FPGA connection blocks (CBs) are only used for connecting the logic cluster. So generally more than 70 percent of the total available logic area is consumed by interconnection where the rest is consumed by logic during algorithm computation. So we modify the exiting circuits of CBs to a new architecture of connection blocks (CBs) which can work in both modes, as logic computation unit or as routing.

The main advantages offered by hybrid architecture are computation speed, logic concentration and power utilization.

- **Computation Speedup**

In order to raise the algorithm computation speedup, the concentration of the circuit must be reduced. There are three primary definitions of speed depending on the context of the problem: throughput, latency, and timing. In the context of processing data in an FPGA, throughput refers to the amount of data that is processed per clock cycle. A common metric for throughput is bits per second. Latency refers to the time between data input and processed data output. The typical metric for latency will be time or clock cycles. Timing refers to the logic delays between sequential elements. When we say a design does not "meet timing," we mean that the delay of the critical path, that is, the largest delay between flip-flops (composed of combinatorial delay, clock-to-out delay, routing delay, setup timing, clock skew, and so on) is greater than the target clock period. So as we know CPLDs (PLA) are characteristically faster in computation and have more predictable timing than FPGAs(LUTs) so for the large fan in application, we utilize the connection block circuit in PLA mode to maximize the computation speedup of hybrid circuit.

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- **Logic Concentration:**

With the integration of the FPGA and CPLD technology and logic circuits, the area of the chip is decreased. Circuit-level reduction as performed by the synthesis and layout tools refers to the minimization of the number of gates in a subset of the design and may be device specific. Preliminary results indicate that compared to LUT-based FPGAs the Hybrid offers savings of more than a factor of two in terms of chip area. As we know FPGAs are generally denser and contain more flip flops and registers than CPLDs. If we execute an application with HRCA then logic circuit can be configured as either PLAs or LUTs mode according to number of inputs (fan-in). In this mechanism we reduce architectural area of proposed architecture as compare to regular FPGA. Proposed hybrid architecture design show that significant chip area is reduced using this architecture approach and optimization [17] (Fig. 3)

- **Power Optimization**

FPGAs are power-hungry beasts and are typically not well suited for ultralow-power design techniques. A number of FPGA vendors do offer low-power CPLDs (complex programmable logic devices), but these are very limited in size and capability and thus will not always fit an application that requires any respectable amount of computing power. HRCA will offer significant savings in power consumption in the circuit by using a proper mix of CPLD and FPGA techniques.

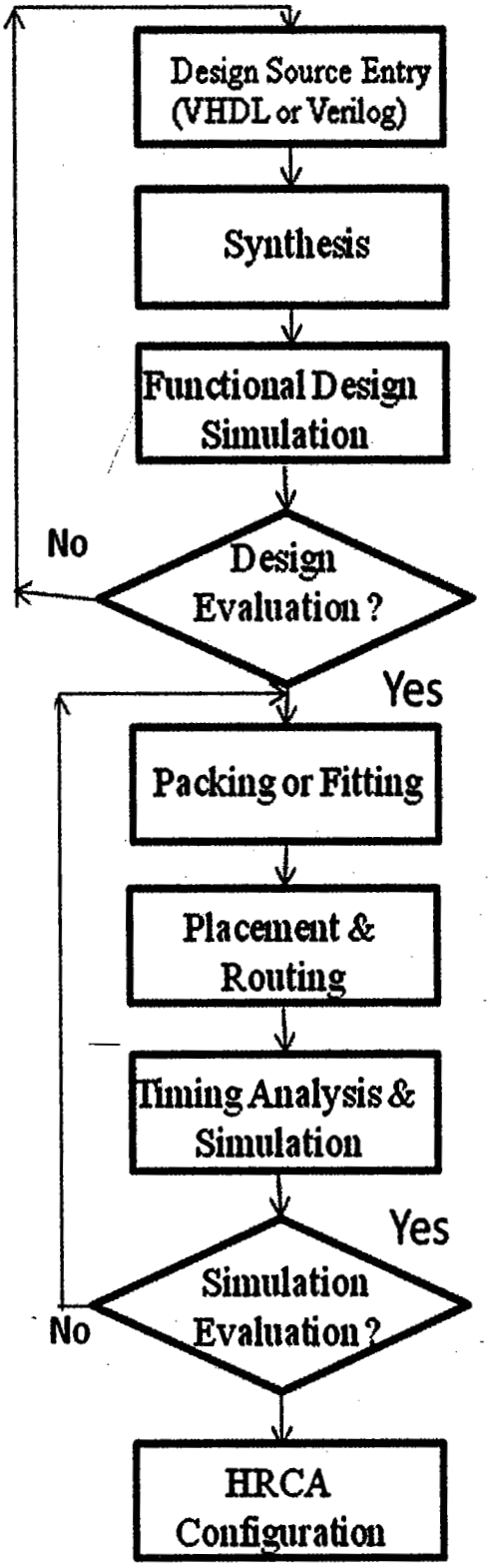

Figure 3: CAD optimization of HRCA

In CMOS technology, dynamic power consumption is related to charging and discharging of parasitic capacitances on gates and metal traces.

The general equation for current dissipation in a capacitor is

$I = V * C * f$

where I is total current, V is voltage, C is capacitance, and f is frequency. Thus, to reduce the current drawn, we must reduce one of the three key parameter. In Hybrid FPGA design, the voltage (V) and frequency (f) are usually fixed. This leaves the parameters C to manipulate the current. The capacitance (C) is directly related to the number of gates that are toggling at any given time and the lengths of the routes connecting the gates and registers. As we know that FPGAs are generally denser and contain more logic gates and registers than CPLDs. So power consumption is more in FPGA than CPLD. So Hybrid FPGA show remarkable power saving as compared to the traditional FPGA containing with only LUTs.

7. CONCLUSION

We have reviewed the factors which determine the performance of hybrid architecture namely speed, area and power. Techniques to increase the performance of the hybrid reconfigurable systems are explained. We then discussed some of the hybrid architectures that have been proposed and studied their performance based on these three factors. In our study we notice that the integration of FPGA technology with PLAs shows considerable improvement in terms of area reduction, speed-up performance and power optimization. In future, we would be evaluating the runtime area optimization and performance approach of our proposed HRCA with traditional FPGA using MCNC benchmarks circuit. MCNC benchmarks circuit are very popular in academic research.

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