Design Of CMOS Analog Signal Multiplier Using Differential Difference Current Conveyor

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Abstract

This paper presents a research work on an analog signal multiplier with a current conveyor. With the advancement in technology, the number of transistor per unit area of chip has been increasing. As the number of transistor increases, the number of nodes in the system will also increase. Since the signal passing through any system drops at each node, the resultant drop of signal will also increase with the increase in the nodes. This problem can be countered with a current mode signal processing. This signal processing will give better results as compared to voltage mode signal processing like large gain, more linearity, higher slew rate etc. Here we propose a current mode circuit, called current conveyor, for designing a multiplier instead of an operational amplifier. Simulation results of this multiplier circuit show better results as compared to an op-amp multiplier in terms of gain, linearity, slew- rate etc. The proposed building block introduces a technique, based on a current-conveyor, suitable for the design of high frequency bandwidth analogue multipliers. The differential difference current conveyor has better linearity, gain & bandwidth with a differential input facility as compared to other current conveyor circuit like CCI, CCII, etc. The Full-Differential CMOS Analog Multiplier Current Conveyors, designed using tanner tool, has a rail-to-rail voltage of ±1.5 volt and a 120 MHz bandwidth in a 0.5 um technology. The power consumption is about 3.2mW from a ±1.5V power supply voltage, and the total harmonic distortion is 0.98 % with a 1V input signal.

Key Words: CMOS, DDCC, multiplier, op-amp

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1. Introduction

A novel circuit for an analog multiplier in a standard CMOS process is described. It is based on a two-current conveyors cell associated with a four MOSFET transconductor.

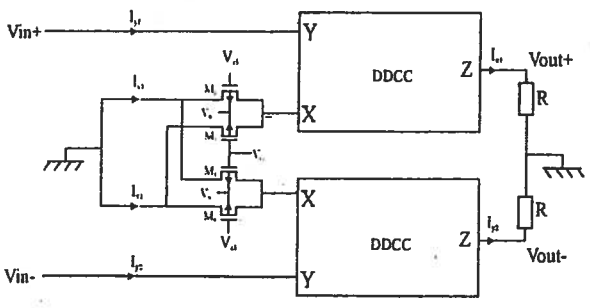

Fig: 1 Block diagram a four-quadrant multiplier

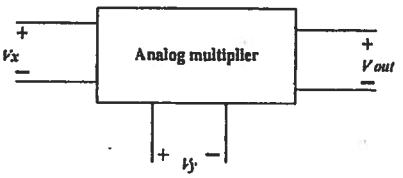

Fig: 2 Block diagram of an analog Multiplier

This differential multiplier achieves a higher bandwidth as compared to conventional or OP-AMP based multiplier, because of the use of high-frequency current conveyors. This multiplier is termed a four-quadrant multiplier because both inputs can be either positive or negative. The ideal output of the multiplier is related to the inputs by

$Vout$ =Km VxVy (1.1)

where Km is the multiplier gain with units of V-I. In reality, imperfections exist in the multiplier gain, resulting in offsets and nonlinearities. The output of the multiplier can be written as

$Vout = Km\ (Vx + Vosx)(Vy + V\ osy) + V\ osout + Vx'' + Vy$ (1.2)

where $Vosx'$ $Vosy'$ and $Vosout'$, are the offset voltages associated with the x-, y-inputs, and the output, respectively. The terms Vx'' and Vy''' represent nonlinearities in the multiplier. Normally, these nonlinearities are specified in terms of the total harmonic distortion. In applications such as analog signal processing, automatic control, and instrumentation systems, processing differential voltage signals is very common, thus a single voltage input terminal is hardly competent. This problem can be eliminated by DDCC. By using the differential properties of differential difference conveyor and other properties of current conveyor we can make a multiplier that has better gain with maximum linearity and minimum distortion.

1.1. Current Conveyor

The current conveyor (CC), as initially introduced, is a 3-port device whose black box representation can be seen in fig. 3.

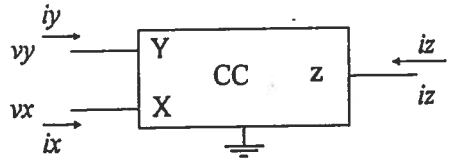

Fig. 3. Block representation of the current conveyor.

The operation of this device is such that if a voltage is a applied to input terminal Y an equal potential will appear on the input terminal X. In a similar fashion, an input current I being forced into terminal X will result in a equal amount of current I will be conveyed to output terminal Z such that terminal Z has the characteristics of a current source, of value I, with high output impedance. As can be seen, the potential of X, being set by that of Y, is idenpendent of the current being forced into port X. Similarly, the current through input Y, being fixed by that of X, is independent of the voltage applied at Y. Thus the device exhibits a virtual short-circuit input characteristic at port X and a dual virtual open-circuit input characteristic a port Y.

Design of DDCC

Conventional current conveyors like CCI and CCII have an apparent disadvantage of having only one input terminal. The DDCC have advantages of a multi input terminal with a differential input property.

The DDCC is a versatile building block for implementing differential and floating input circuits. Furthermore, the other current conveyors, such as CCII, CCIII, ICCII (Inverting Second Generation Current Conveyor), and DVCC (Differential Voltage Current Conveyor) can be easily obtained by using DDCC. In the proposed circuit, we introduce the negative feedback action to reduce channel length modulation effect of MOS transistors. Thus, it has less harmonic distortion and large linear dynamic range. SPICE simulations confirm the excellent properties of the proposed circuits

The DDCC is a six-port building block as shown in Fig 2.11. It has three voltage input terminals: Y1, Y2 and Y3, which have high input impedance. Terminal X is a low impedance current input terminal. There are two high impedance current output terminals: Z+ and Z-. The input-output characteristic of the DDCC is defined as:

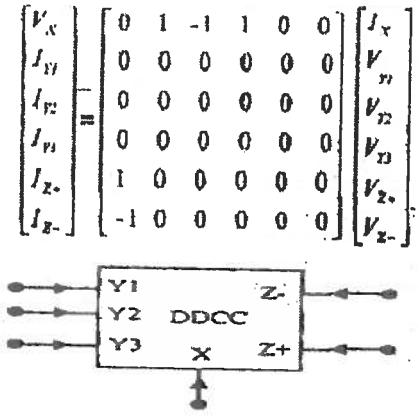

Fig 4. Symbol of DDCC

The output currents *(Iz+* and *Iz.)* follow the input current through terminal X. *Iz+* has the same polarity as *Ix,* and *Iz-* is in the opposite polarity as *Ix.* The voltage of X terminal is related by the three inputs voltage:

$Vx=Vy_1-Vy_2+Vy_3$.

The proposed CMOS realization of DDCC is shown below

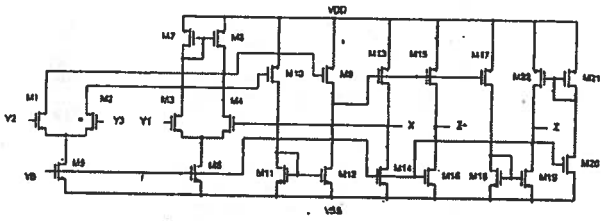

Fig. 5 CMOS Differential Difference Current Conveyor

All transistors operate in the saturation, and their bulk is connected to the appropriate positive or negative supply rail.

1.2. Derivation of formulas for DDCC

Assuming that M7 and M8 are matched, the current mirror formed by transistors M7 and M8 forces the sum of drain currents of MI and M3 to be equal to the sum of the drain currents of M2 and M4, hence

$$I_7=I_8=I_2+I_3=I_1+I_4 \qquad (1.4)$$

Therefore,

$$I_1-I_2=I_3-I_4 \qquad (1.5)$$

Because the differential output current of the differential pair is a monotonous function of differential input voltage I, the following expression can be obtained

$$V_{Y2}-V_{Y3}=V_{Y1}-V_X \qquad (1.6)$$

$$V_X=V_{Y1}-V_{Y2}+V_{Y3} \qquad (1.7)$$

Therefore, except M_1-M_4, all the MOSFETs have sources that are connected to the positive or negative supply rail. Thus there is no threshold voltage variation caused by the body effect. Because the transistors (M_1 and M_2) have equal variation in the threshold voltage caused by the body effect, the threshold voltage variation can be canceled out. The same is true for the differential pair M3 and M4. Therefore, the circuit is insensitive to the threshold voltage variation caused by the body effect.

We assumed that I_7 equals to I_8. If V_{D8}, is not equal to V_{D7} the channel length modulation effect of the MOS transistors will cause a current error. In the proposed DDCC, the transistors M_9-M_{12} are used to reduce this current error. Because transistors M_9 and M_{10} have the same device size, the current mirror formed by transistors M_{11} and M_{12} forces V_9 to become equal to V_{G10}.

The transistors M_9 and M_{13} provide negative feedback to make the voltage Vx less dependent on the current drawn from the terminal X. The current through terminal X is conveyed to Z+ terminal by the current mirrors, which consist of transistors M13, M15, & M16. By using extra current mirrors, current through terminal X is conveyed to Z- terminal with the negative polarity.

2. The multiplying quad

The multiplication is performed by a four MOSFET differential configuration shown above in the figure. The major interest of this

approach is the implementation of an ac linear resistor without distortion due to the bulk-source voltage. This realization is a true floating resistor. By assuming that all the devices are matched and are in the ohmic region, an expression for the ac resistor can be obtained as follows

$$G=\frac{I1-I2}{V1-V2}=K\frac{W}{L}(V_{C1}-V_{C2}) \quad (2.1)$$

where K is given by,

$$K=u.C_{ox} \quad (2.2)$$

Parameters u and C_{ox} are respectively the average carrier mobility in the channel and the gate oxide capacitance per unit area. L and W are respectively the length and the width of the transistor. Relation (1.1) is true if the conditions

$$V_1, V_2 < \min[V_{C1}-V_T, V_{C2}-V_T] \quad (2.3)$$

are verified, where V_T is the threshold voltage.

3. Simulation results:

Fig.9 shows the application of the multiplier as an amplitude modulator. The modulation is

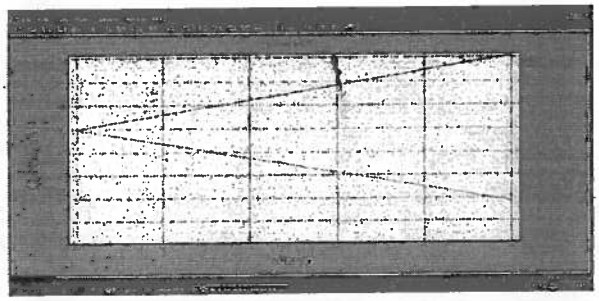

Fig: 6 Current for z+ , z- & x terminal

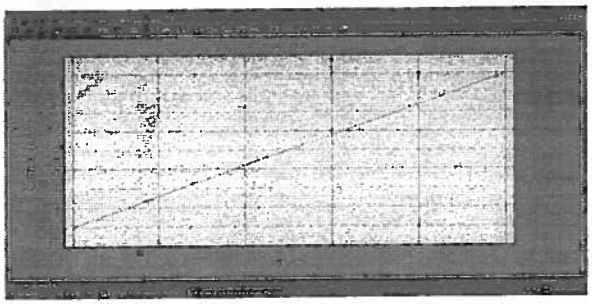

Fig:7 Current waveform for M5 & M6 transistors.

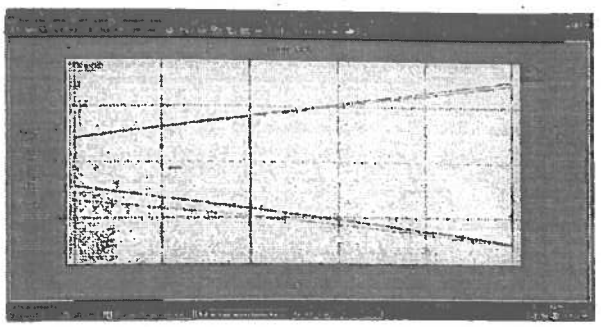

Fig: 8 Current waveform for current mirror M18,M19 M21,M22.

Table: transistor aspect ratio of DDCC

Transistors	W/L(um)
M1-M4	1.4/0.5
M5-M6	37/0.5
M7-M12	18/0.5
M13, M15, M17	34/0.5
M14, M16, M18	65/0.5
M21M22	26/0.5
M19M20	65/0.5

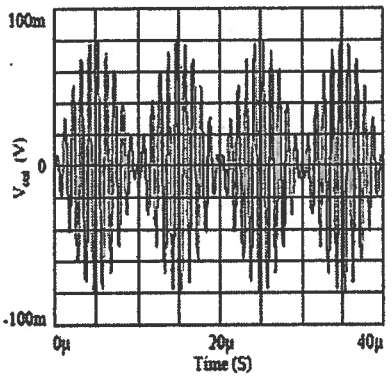

Fig:9 Amplitude modulation of sinusoidal signal

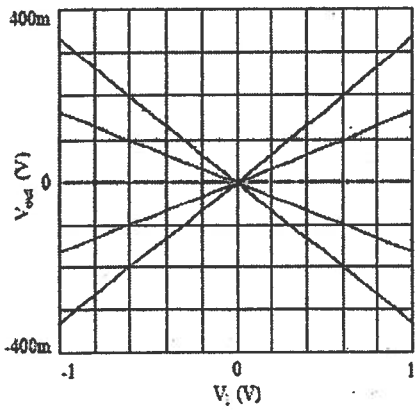

Fig:10 Transfer characteristics of the multiplier

performed when the input voltage $V1$ and $V2$ are the 1MHz and 50kHz sinusoidal input signals with peak amplitude of 0.5V. The frequency characteristic of the multiplier is measured, where a dc voltage of 1V is applied to $V2$ while $V1$ is the variable frequency. From the result, the -3dB bandwidth of 85MHz is achieved.

5. Conclusion

A CMOS Analog Signal Multiplier Using Differential Difference Current Conveyor (DDCC) has been designed by using hp 0.5µm CMOS process. The circuit is based on non-linearity characteristic of a simple differential pair that achieves the output signal in voltage form without using resistors. This multiplier circuit gives a 85 MHz bandwidth. The performances have been demonstrated by using T-SPICE.

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