A NOVEL ACTIVE SHUNT-PEAKED MCML ARRAY MULTIPLIER

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ABSTRACT

In this paper, a new architecture for MOS Current Mode Logic (MCML) array multiplier for mixed-signal applications is proposed. The proposed architecture employs active shunt-peaking technique in conventional MCML circuits. The technique of active shunt-peaking offers a way for increasing the speed of MCML gates. The performance of the proposed MCML array multiplier is compared with the conventional one through SPICE simulations by using 0.18µm TSMC CMOS technology parameters. It is found out that the proposed array multiplier shows an improvement of 31 percent in the values of delay parameters in comparison to the conventional MCML design.

Key word: *Current mode logic, shunt-peaking, array multiplier.*

I. INTRODUCTION

The recent developments in VLSI technology have allowed rapid growth in the area of mixed-signal integrated circuits (ICs) [1-2]. These ICs contain analog and digital circuits on the same chip. Traditionally, CMOS logic style is the best option for designing digital circuits due to the rail-to-rail voltage swing and no static power consumption. But in mixed-signal applications the traditional CMOS logic style is not suitable as it generates large switching noise which limits the resolution of analog counterparts on the same chip [3]. Many techniques to reduce the switching noise of the digital circuits have been proposed in literature [4-12]. Out of them the most promising one is the MOS Current Mode Logic (MCML) to design digital circuits. They exhibit high switching speed, high noise immunity and better power efficiency at high operating frequencies with a drawback of static power consumption [12-14].

In mixed-signal applications, digital circuits are extensively used in the realization of digital signal processor functional units such as Finite Impulse Response (FIR) filter and FFT module. The module requires extensive sequences of multiply-and-accumulate computations. Hence, a multiplier is a key element in such modules. In this work, a high speed realization for an array multiplier for mixed signal applications is proposed. The proposed structure employs active inductors and use shunt-peaking technique to increase the speed of the multiplier. The technique was originally demonstrated for analog and RF applications but it can be easily applied to the design of high-speed MCML gates because of the characteristics mentioned above.

The paper begins with a brief introduction to conventional MCML circuits in section II. In the next section III, the technique of active-shunt peaking is explained and is applied to MCML circuits. Section IV proposes the architecture and circuits of the array multiplier. The proposed multiplier is implemented, simulated and the results are discussed in section V. Finally, the paper is concluded in section VI.

II. MCML CIRCUITS

The conventional MCML circuit is differential in nature. It consists of three main components which include a pull-down network (PDN), a current source and resistive load. The PDN realizes the logic

function by using the series-gating approach. The logic function implementation may contain either single or multiple levels of source-coupled transistor pairs. The constant current source determines the source current, I_{ss} whereas the load circuit, R_L determines the voltage swing, $V_{SWING.}$

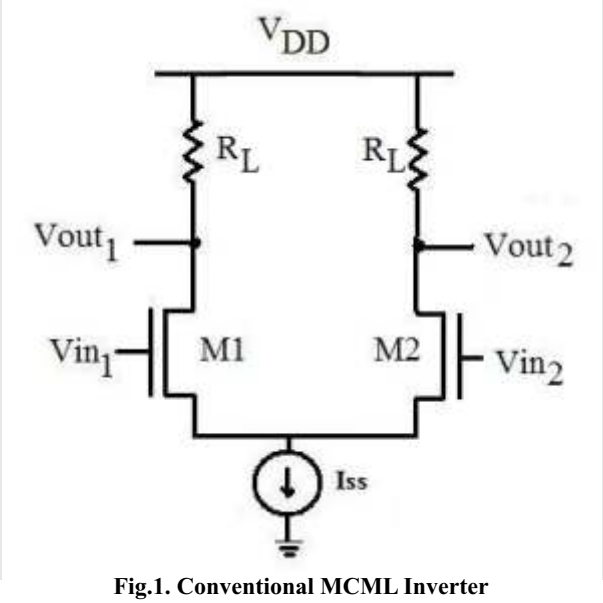


Fig.1. Conventional MCML Inverter

The circuit of a conventional MCML inverter with a source coupled transistor pair (M1, M2) in the PDN is shown in Fig. 1. The circuit works on the principle of current steering. For a high value of the differential input voltage ($V_{id} = V_{in1}-V_{in2}$), the bias current, I_{SS} is steered to transistor M1 and a low differential output ($V_{OL}= V_{out1}-V_{out2} = -I_{SS}R_L$) voltage is obtained at the inverter output. Similarly for low differential input voltage, the bias current I_{SS} gets steered to transistor M2 and thus a high differential output ($V_{OH} = V_{out1}-V_{out2} = I_{SS}\ R_L$) is obtained at the inverter output. Thus, these circuits are characterized with a reduced voltage swing, V_{SWING} given as:

$$V_{SWING} = V_{OH} - V_{OL} = 2 R_L I_{SS} \quad .....(1)$$

III. ACTIVE SHUNT-PEAKING TECHNIQUE

The speed of the conventional MCML circuit can be improved by using shunt-peaking technique. This technique in a common source amplifier resulted in a 50% increase in the on-chip bandwidth [15]. It involves the use of a spiral inductor in series with the load resistor at the output node in order to convert a first-order RC network to a second order under-damped RLC network. The use of the spiral inductor has several limitations such as large component size and lengthier design process. As a result, active inductor is used in place of spiral inductor to eliminate these limitations. An active inductor requires at least one active device that behaves as an inductor for small-signals. A simple active inductor topology proposed by Worapishel et.al [16-17] is shown in Fig. 2a. It consists of an NMOS transistor, ML1 and a resistor, R_bias (1/G) connected to its gate. The small-signal model for the active inductor is shown in Fig. 2b.

The equivalent impedance of the active inductor is

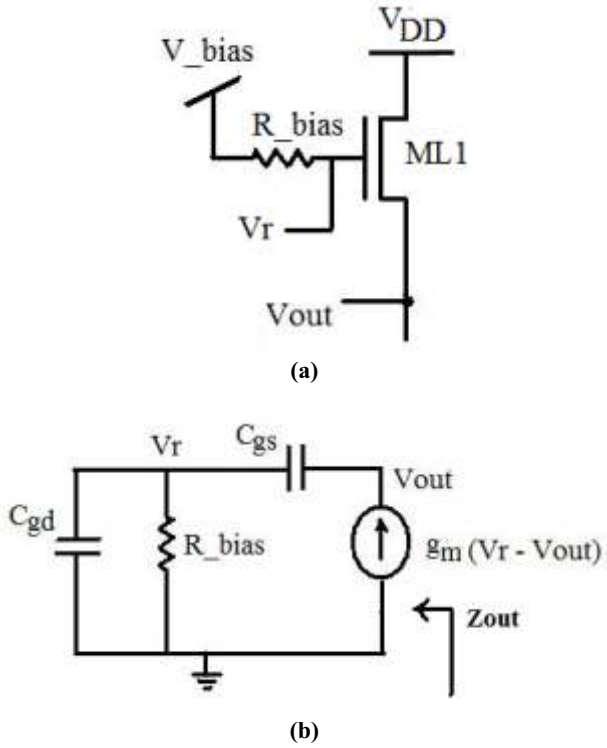


Fig.2. a) Active inductor [16] b) its simplified s small-signal equivalent.

computed as

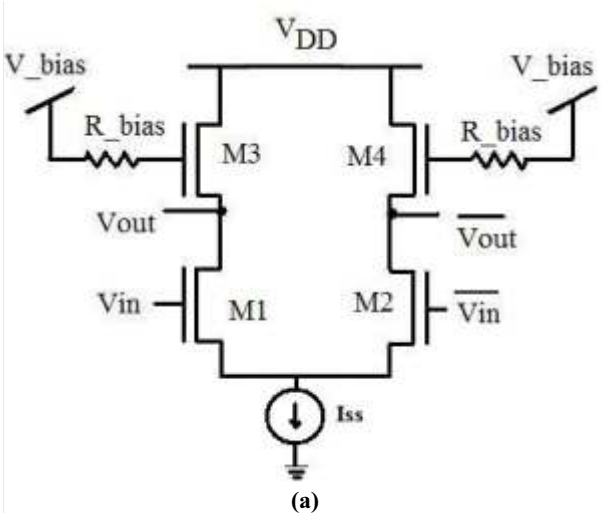
$$Z_{out} = \frac{s(C_{gd} + C_{gs}) + G}{s^2 C_{gd} C_{gs} + s(C_{gs} G + C_{gd} g_m) + g_m G} \quad ....(2)$$

(2)

Where C_{gd}, C_{gs} are the gate-drain capacitance, gate-source capacitance of the transistor ML1 and g_m is

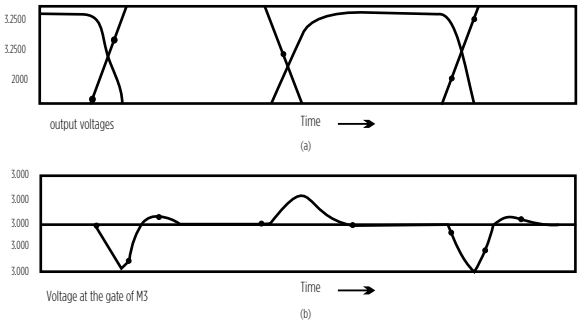
the
transconductance of the transistor. The transfer function in (2) has two poles and a zero. The zero in the transfer function is responsible for increasing the speed of the gates.

In conventional MCML circuit, active shunt-peaking can be achieved by replacing the load resistor with the above inductor. These circuits are known as active-shunt peaked MCML circuits and may be abbreviated as MCML-SP circuits. The circuit of a MCML-SP inverter is shown in Fig. 3a. When a positive (L-H) transition occurs at the output node (Vout), the charges gets coupled to the gate the transistor M3 through gate-source capacitance (c_{gs}) which in turn increases the gate potential of transistor M3. The injected charges do not disappear immediately due to the presence of resistor (R_bias). Thus, a gate-source voltage which is larger than the case when the gate was connected to a fixed potential is produced. The increased gate-source voltage increases the drain current of transistor M3 which enhances the charging of output node Vout and decrease the switching time. Similarly, a negative transition (L-H) at the inverter output withdraws the charges from the gate of M3 and the drain current of M3 decreases faster and supports the discharging of the inverter output node. The transient response of an MCML-SP inverter is shown in Fig. 3b. The upper waveform shows the input output waveforms of the inverter whereas the lower waveform demonstrates the phenomenon of active shunt peaking through the



(a)

change in gate potential of M3 during transitions.



(b)

Fig.3.a) MCML-SP inverter b) Transient Response of a MCML-SP inverter.

IV. ARRAY MULTIPLIER

An array multiplier is a combinational circuit that employs an array of adders and AND gates. An adder is used to perform the addition of the bits produced by the AND gates. A block diagram of a 2-bit array multiplier is shown in Fig 4. It consists of four AND gates (X1-X4) and two half adders (HA1, HA2)

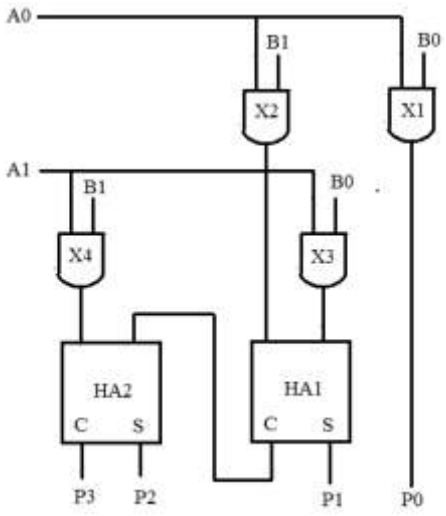
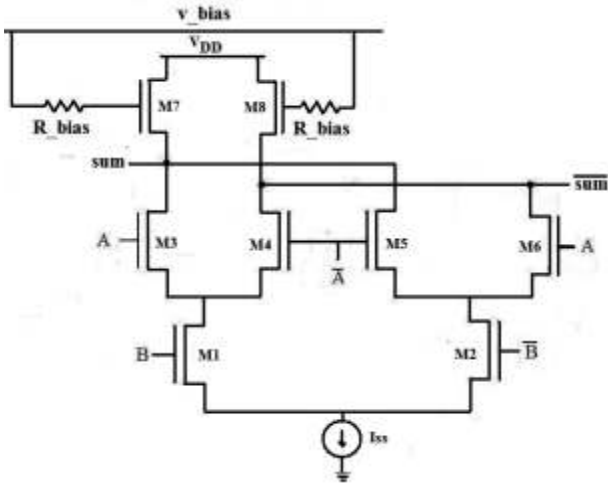


Fig.4. Block diagram of a 2-bit array multiplier

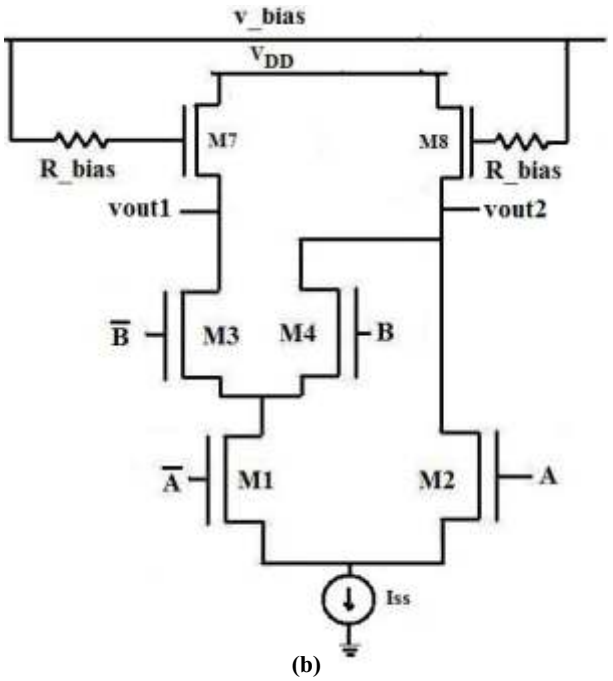
wherein the carry is propagated serially.

Fig. 5 shows the implementation of the proposed sum and carry circuit for a half adder. The sum circuit is implemented in Fig.5a by realizing the minterms separately and then performing the OR operation by simply connecting the drain of transistor M3 and M5. The carry operation is obtained by stacking two source coupled pairs as shown in fig 5b. When both the transistors M1-M3 are on, the bias current I_{ss} gets steered through them and a low voltage is produced at the corresponding output branch.

Fig. 6 shows the implementation of the proposed MCML-SP sum and carry circuits in a full adder. The sum and carry circuits employs a three input exclusive OR (XOR) and a majority (two out of three) respectively. The PDN of the sum in Fig 6a is a binary tree-like, three-level MCML circuit with a carry input at the bottom, the signal B in the middle and signal A at the top level. This topology lowers the



(a)

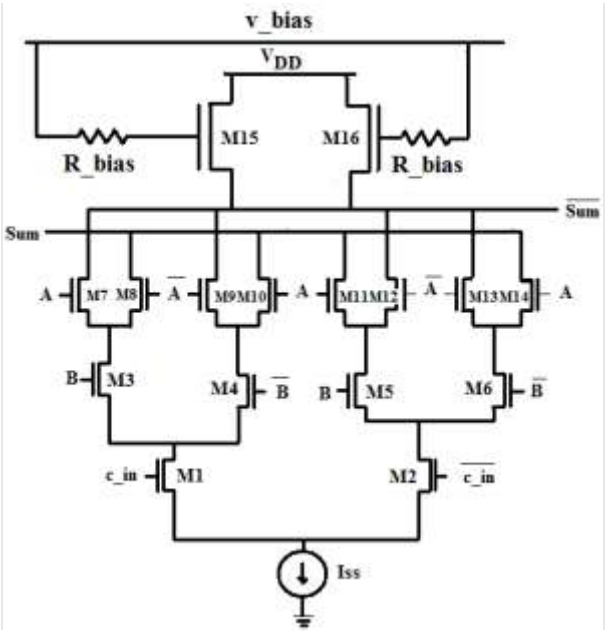


(b)

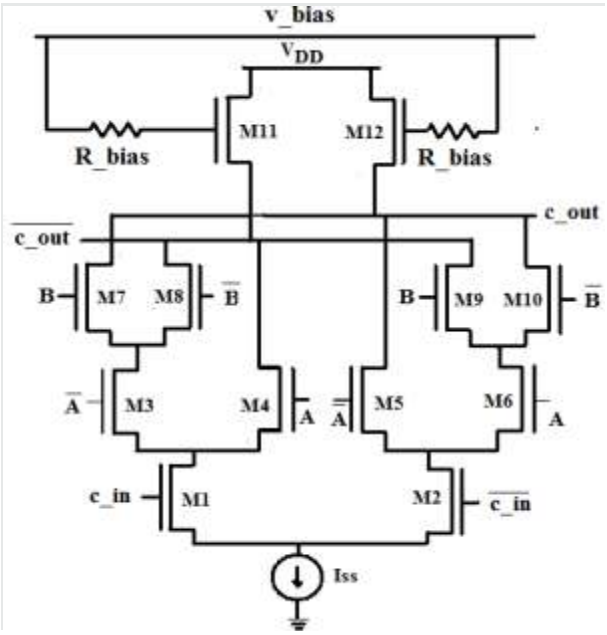
Fig.5. Proposed MCML-SP half adder a) sum circuit b) carry circuit

load capacitance on the first stage [18].

The MCML-SP carry circuit in Fig.6b has a carry (c_in) connected to the bottom transistors in PDN which minimizes the delay during worst-case



(a)



(b)

Fig. 6 MCML-SP full adder a) sum circuit b) carry circuit

analysis.

V. SIMULATION RESULTS

In this section the simulation results for the sum and carry circuits in half and full adders are first presented. Thereafter the results for the proposed MCML-SP array multiplier are reported. All the circuits are simulated using 0.18 μm TSMC CMOS process parameters. The input parameters taken in the simulations are listed in Table I.

Table I

Simulation Environment

Simulation Environment	
Process Corner	Typical
Temperature	27 °C
Supply Voltage	1.8 V
Clock Frequency	500 MHz
Data/Clock rise/fall time	10% of T_{clk}
Bias Current	100 uA

The sum and carry circuit shown in Fig 5 and 6 are simulated to test the effectiveness of the proposed technique. For the purpose of fair comparison, the conventional MCML sum and carry circuits are also simulated. The results for power consumption and delay such as rise time, fall time, propagation delay are tabulated in Table II and III. It can be observed that the power results for the conventional MCML and the MCML-SP circuits are equal. This is due to the fact that both of them have the same bias current and hence consume equal static power. In terms of delay, the MCML-SP adders have reduced values due to the active shunt peaking technique. An improvement of 22 percent in the propagation delay can be observed in MCML-SP circuits in comparison to conventional MCML circuits. The simulation results for the array multiplier are reported in Table IV. The results indicate that the proposed MCML-SP array multiplier is faster than the conventional MCML multiplier by 31 percent.

VI. CONCLUSION

This paper presents the use of active shunt-peaking technique in MCML gates. An array multiplier based on active shunt-peaking technique has been proposed. It is found that the proposed multiplier is faster than the conventional MCML multiplier while maintaining the desired digital characteristics. The analysis of the simulated results confirms the feasibility of the active shunt-peaking technique in array multiplier and shows that there is an improvement up to 31 percent in the value of delay parameters as compared to the conventional MCML circuit.

Table II

Summary of simulated performance for a Half adder

Simulation Parameter	Sum		Carry	
	Conventional MCML	MCML-SP	Conventional MCML	MCML-SP
Power (uW)	180	180	180	180
Propagation Delay (ps)	122	100	93	85
Rise Time (ps)	358	346	310	290
Fall Time (ps)	387	349	370	340

Table III

Summary of simulated performance for a full adder

Simulation Parameter	Sum		Carry	
	Conventional MCML	MCML-SP	Conventional MCML	MCML-SP
Power (uW)	180	180	180	180
Propagation Delay (ps)	140	120	246	240
Rise Time (ps)	670	600	563	583
Fall Time (ps)	810	750	520	530

Table IV

Summary of simulated performance for a 2-bit Array multiplier

Simulation Parameter	Sum		Carry	
	Conventional MCML	MCML-SP	Conventional MCML	MCML-SP
Power (uW)	180	180	180	180
Propagation Delay (ps)	181	148	490	420
Rise Time (ps)	175	172	745	665
Fall Time (ps)	486	369	721	660

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